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AN INVESTIGATION OF MOS CAPACITOR PULL-UP CIRCUITS

by


A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of

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Faculty of Engineering

Carleton University

Ottawa, Ontario

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The undersigned recommend to the Faculty of Graduate Studies and Research acceptance of the thesis:

AN INVESTIGATION OF MOS CAPACITOR PULL-UP CIRCUITS

submitted by Joseph Paul Ellul in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

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Thesis Supervisor

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1976
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ABSTRACT

The use of an MOS capacitor as an integrated load element in dynamic inverters is reviewed and a particular approach (direct cascading) to its application is demonstrated. Experimental n-channel capacitor pull-up shift registers are demonstrated to operate with multi-phase clocks at frequencies up to 34.5 MHz which is about twice the limit of conventional MOS dynamic circuits fabricated with the same Si-gate process. A substrate bias is used to eliminate minority carrier injection which was previously reported to limit the high frequency performance.

A novel two-level self-aligned polysilicon-gate process is developed for designing and fabricating higher performance capacitor pull-up circuits. Computer simulation results show a marked improvement in the performance of capacitor pull-up one-bit shift registers implemented with the developed process. Discussions on system applications show that capacitor pull-up circuitry is capable of very high frequency operation (>60 MHz) and low power dissipation. A 1024-bit shift register requires 23 mW at 1 MHz. Comparisons to other circuits are made and possible further work is discussed.
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<td>$C_{ox}$</td>
<td>Gate-oxide capacitance per unit area</td>
</tr>
<tr>
<td></td>
<td>$V_{BS}$</td>
<td>MOST back-gate bias (substitute bias)</td>
</tr>
<tr>
<td>2.6</td>
<td>$L$</td>
<td>MOST gate length</td>
</tr>
<tr>
<td>3.2</td>
<td>$T$</td>
<td>Clock pulse period</td>
</tr>
<tr>
<td></td>
<td>$V_{min}$</td>
<td>Minimum clock pulse height</td>
</tr>
<tr>
<td></td>
<td>$V_{p}$</td>
<td>Peak negative drain potential</td>
</tr>
<tr>
<td>4.2.2</td>
<td>$C_D$</td>
<td>Parasitic surface depletion capacitance</td>
</tr>
<tr>
<td></td>
<td>$C_{F1INV}$</td>
<td>Parasitic field induced junction capacitance</td>
</tr>
<tr>
<td>SECTION</td>
<td>SYMBOL</td>
<td>Definition</td>
</tr>
<tr>
<td>---------</td>
<td>--------</td>
<td>-----------</td>
</tr>
<tr>
<td>4.2.2</td>
<td>$C_{F0}$</td>
<td>Parasitic field oxide capacitance</td>
</tr>
<tr>
<td></td>
<td>$C_j$</td>
<td>Parasitic diffusion junction capacitance</td>
</tr>
<tr>
<td>4.2.3a</td>
<td>$C_{jA}$</td>
<td>Diffusion junction area capacitance</td>
</tr>
<tr>
<td></td>
<td>$C_{jP}$</td>
<td>Diffusion junction peripheral capacitance</td>
</tr>
<tr>
<td>5.2.1</td>
<td>$C$</td>
<td>Capacitance</td>
</tr>
<tr>
<td></td>
<td>$C_o$</td>
<td>Maximum value of oxide capacitance</td>
</tr>
<tr>
<td></td>
<td>$N_{D0}$</td>
<td>Original doping concentration in Poly 0 electrode</td>
</tr>
<tr>
<td></td>
<td>$N_{D1}$</td>
<td>Doping concentration in Poly 0 electrode after oxidation</td>
</tr>
<tr>
<td></td>
<td>$N_{D2}$</td>
<td>Doping concentration in Poly 0 electrode after final high temperature processing steps</td>
</tr>
<tr>
<td></td>
<td>$\Delta V$</td>
<td>Voltage shift in capacitance curves</td>
</tr>
</tbody>
</table>
CHAPTER 1

INTRODUCTION

1.1 HISTORICAL INTRODUCTION

This thesis investigates the use of an MOS capacitor as an integrated circuit load element in dynamic MOS LSI logic circuits. This possibility was first mentioned in a paper by Luscher and Hofbauer [1], in 1966, in their attempt at making frequency dividers with very low power consumption while maintaining simplicity of structure and ease of fabrication. Later, Krebs and Ryder [2] described the use of such a load for inverters in circuits employing two or more clock phases. This was followed by a paper by Crawford and Bazin [3] in which the analysis of this new circuitry was considered in detail. Figure 1.1 shows the schematic of a capacitive-load shift register bit used by Crawford and Bazin in their analysis. The circuit had a transmission gate, driven by the same clock, in series with the inverter. This transmission gate samples the output level of the inverter and holds the logic state on the input of the following stage. The shift register requires two-phase non-overlapping clocks with two inverters and two transmission gates per bit. Shift registers were built and successfully operated using a p-channel, metal-gate process. Theoretical calculations showed that the upper speed limit of this type of circuit was in the 25-30 MHz range with the technology then available. However, the maximum observed frequency of operation was 5 MHz, with the upper frequency limit attributed to injection of
Figure 1.1. The original proposal of Crawford and Bazin for the capacitor pull-up inverter circuit.

... minority carriers into the substrate which resulted in severe signal degradation.

No further work was published after Crawford and Bazin on capacitor pull-up circuitry.

1.2 PRELIMINARY INVESTIGATION

In September 1972, the author, as part of his M.Eng. Thesis, started a preliminary investigation of the speed capability of capacitor pull-up MOS dynamic logic and its overall suitability for LSI circuit design [4]. The investigation involved the breadboarding of
Figure 1.2. The circuit schematic of the dynamic capacitor pull-up inverter used with overlapping clock pulses.

capacitor pull-up inverters, among other things, in the manner shown in Figure 1.2. Here, the load capacitor, \( C_L \), replaced the load transistor in the more conventional MOS logic circuits. Logic levels are obtained with capacitor divider action between \( C_L \) and the MOST drain capacitor, with the MOST acting as an ON/OFF switch allowing for the capacitors to maintain a charged state or to discharge to ground.

Both p-channel and n-channel discrete MOSTs were utilized for the inverter driver transistor, \( Q \). A computer program was written, using the TSL program Simul 8*, and hence simulated results were obtained for the inverter operation. By changing the values of the discrete

* This program is available in the Computing Centre facilities of Carleton University
capacitor $C_L$, various experimental results were obtained. The simulated results compared favourably with the experimental results. One of the main observations was that an optimum operating condition was for the capacitor divider ratio to be set equal to $1/2$. For this ratio, the discharge time of the capacitors was minimum. The investigation was extended to bit delays achieved by the direct cascading of four inverters and the use of overlapping clock pulses. Also, in the context of a general logic application, a modulo-8 counter was successfully breadboarded with discrete devices.

Since the investigations of capacitor pull-up circuits using discrete devices proved promising, an attempt was made to design an integrated version of a shift register by cascading a few one-bit delays. The process chosen was an n-channel silicon-gate process. Two separate circuits were designed. One was a 10-bit shift register with one serial input and 10 parallel outputs. This was designed so as to allow the characterization of each bit delay separately. The other integrated circuit was a 16-bit shift register with one serial input and one serial output. Based on these designs, approximate theoretical results were presented and expected frequency limitations were discussed. This formally concluded the author's M.Eng. Thesis.

The two ICs were subsequently fabricated and form part of the continuing work of this thesis.

1.3 PURPOSE OF THESIS

As a result of the investigations reported in the M.Eng. thesis, the capacitor pull-up circuit, using the configuration of Figure 1.2, was seen to have significant advantages over the configuration of
Crawford and Bazin. In particular, the inverter could be much smaller because of the absence of charge-sharing problems, i.e., the capacitance $C_1$ in Figure 1.1 must be large enough so that when charge is distributed between $C_1$ and $C_2$, the output signal is still large enough to drive the transistor $Q_3$. Further, the problem of charge injection to the substrate is much more complicated in the configuration of Crawford and Bazin.

The preliminary work established that the capacitor pull-up inverter, in the configuration of Figure 1.2, is potentially capable of very high-speed and has an overlapping clock requirement which is more suited to high-speed operation than the clocks used by the more common dynamic MOS LS1 circuits.

The purpose of this thesis was therefore to carry forward the development of the circuit technology and process technology of capacitor pull-up circuits to the point where the potential advantages of speed and simplicity of operation could be realized and to attempt to investigate and hopefully overcome the limitations of the circuit, particularly in terms of the area required to implement it.

1.4 THESIS SUMMARY

Chapter 1 contains the introduction to the thesis. The theory and analysis of capacitor pull-up circuits are described in Chapter 2. The basic model of the integrated capacitor pull-up inverter, as well as all discussions of the design and operation of the devices that are presented, pertain to a standard n-channel silicon-gate process. Computer simulation results are also presented. In Chapter 3, the
experimental results obtained from the shift registers built using the standard n-channel process are presented. In Chapter 4, the basic model presented in Chapter 2 is extended to develop and justify an improved capacitor pull-up process. The basic type of process is sketched and the main differences between it and the standard n-channel silicon-gate process are noted.

Experimental and theoretical results on those parts of the process which depart from standard silicon-gate technology are presented in Chapter 5. On the assumption of such a process, the design of three different shift-registers is discussed. Using standard and measured parameters for the model, computer simulations of the functional behaviour of the circuits are presented. Based on these simulations, a comparison is hence made between circuits designed with the new process and with the standard silicon-gate process.

In Chapter 6, comparisons are made between capacitor pull-up and other circuits, where these are feasible. Applications to general logic are discussed, and the power-delay characteristics of capacitor pull-up inverters designed with the standard silicon-gate n-channel process and with the more optimum process described in Chapter 4 are compared with the power-delay characteristics of $I^2L$ inverters. Conclusions and suggestions for further work are presented in Chapter 7.
CHAPTER 2

THEORY AND ANALYSIS OF CAPACITOR PULL-UP CIRCUITS

2.1 INTRODUCTION

The original motivation for this work was to find a digital logic circuit which operates on the same clocks and the same process parameters as CCD's, to be used for peripheral logic on a CCD chip, saving the necessity for a separate set-up for clocks. However, in the course of this study, it was realized that this logic circuit has general interest also.

A particular approach was used in the present study to exploit the capacitor pull-up circuit. The use of overlapping clocks in the logic circuit removes the requirement for a transmission gate. However, extra stages are needed to obtain signal isolation. By using a suitable substrate bias, the substrate charge injection problem can be avoided. The purpose of this Chapter is to discuss the theory of operation, design and computer simulation of an MOS capacitor pull-up integrated circuit using overlapping clock pulses.

It is useful at this point to discuss the philosophy of the conventional dynamic MOS LSI inverter. Aside from the capacitor pull-up inverter of this thesis, all dynamic MOS LSI inverters operate on a precharge principle, i.e., the inverter is precharged to a high level by charging the load capacitance of the output node through a load transistor or clocked equivalent. The logical output of the inverter is then developed by conditionally discharging the precharged output
node to ground according to the logic input. This technology requires four phases, to allow enough logic levels to perform a general logic.

At least some of the four phase clocks in most types of four phase logic are non-overlapping. This means that the duty cycle of these clocks will be 25%. If one assumes a certain capability of rise and fall time for the clock-generating circuits, it is evident that such clocks cannot be generated cleanly at as high a clock rate as clocks with 50% duty cycle, which are the clocks required by capacitor pull-up circuits (note Figure 2.5).

A major problem of precharge type dynamic logic is that the pre-charge cycle takes time to be achieved, in particular, since the load transistor is generally operating with a much weaker channel than the input transistor. This leads to a longer time constant for the pre-charge than the conditional discharge. Since this precharge cycle is not present in the capacitor pull-up circuit, such a circuit is therefore inherently capable of a higher frequency of operation.

Additional problems of precharge-type MOS logic are caused by the necessity to shield the inverter from the precharge cycle of the previous inverter, until its output is valid, which is time consuming.

The basic capacitor pull-up inverter will be discussed in Section 2.2 with the aid of a simple model. Section 2.3 presents the circuit description and operation of a four-phase shift register one-bit delay. The design of two shift registers using a standard n-channel silicon-gate process is discussed in Section 2.4. Computer simulation results of the functional operation of a one-bit shift register, together with experimental verification, are presented in Section 2.5. Conclusions are discussed in Section 2.6.
Figure 2.1. Schematic of MOS capacitor pull-up inverter.

2.2 THE BASIC Capacitor Pull-Up INVERTER

Figure 2.1 shows a schematic of the basic MOS capacitor pull-up inverter. $C_L$ is the integrated load element capacitor replacing the pull-up resistor in the more common inverter circuit. $C_O$ represents the total capacitance, exclusive of $C_L$, loading the drain, D, of the driver MOST, $Q_1$. The input signal, $V_{in}$, is applied at the gate, G, of the driver transistor. When the clock pulse is applied, capacitive divider action between $C_L$ and $C_O$ results in a potential appearing at node D, which is dependent on $V_{in}$. If $V_{in}$ is high, i.e. $V_{in}$ is greater than the threshold voltage $V_T$, a transient inrush of current from the source brings node D to ground in a time $t_s$, as shown
in Figure 2.2 (curve a). The approximately exponential decay to ground is determined by the transistor channel ON-resistance and the capacitive loading \((C_L+C_O)\), [4]. Hence, a high \(V_{in}\) produces a low \(V_{out}\), i.e. an inverter action. Alternatively, if \(V_{in}\) is low and below threshold, the input MOST is OFF and the rising clock pulls up the potential of the output node according to the capacitive voltage divider ratio \((C_L/(C_L+C_O))\), Figure 2.2 (curve b). Thus, a low \(V_{in}\) produces a high \(V_{out}\), again an inverter action. The shape of the high \(V_{out}\) pulse is similar to the clock pulse, Figure 2.2 (curve c), reduced in height by the capacitive divider ratio. The high output is valid only while the clock is high.
During the clock pulse fall time, the output returns to the original starting voltage if $V_{\text{out}}$ had been high. However, if the output had been low, i.e. grounded, the capacitive action drives the output node below ground. The negative excursion is limited by one of two clamping effects; current flow from the grounded source through the channel of the driver MOST, or, forward current of the substrate-drain diode. The latter is an anomalous mode of operation which usually leads to malfunctioning, as will be discussed later (Section 2.5).

The circuit just described can be identified as an amplifier since it is capable of power gain, derived by drawing power from the clock. This power gain is manifested when the capacitive load at the output is greater than the input capacitance, logic voltage levels being constant.

In a non-self-aligned MOS process, the load element $C_L$ can be fabricated using a diffusion as one electrode of the capacitor, a grown oxide layer as insulator, and a metal gate as the other electrode, Figure 2.3(a). The diffusion mentioned is an extension of the drain diffusion of MOST Q1 in Figure 2.1.

In the self-aligned silicon-gate process, it is not possible to put a gate electrode over a diffusion. However, a capacitor can be achieved functionally through the use of an MOS varactor, where an inverted semi-conductor surface can be the lower electrode of the capacitor. A cross-section of the resulting integrated structure of the inverter is shown in Figure 2.3(b). Under strong inversion, the drain and the area under $C_L$ become one node. When the clock pulse goes on, a potential well is created under the clocked electrode.
Figure 2.3. Integrated structure of MOS capacitor pull-up inverter.
(a) For a metal-gate process
(b) For a silicon-gate process using an MOS varactor as the load element, $C_L$. 
When the input voltage is low, charge from the output (drain) diffusion enters the potential well under the pull-up electrode, giving an effective capacitive voltage divider action. When the input voltage is high, the source, S, grounds the output diffusion in a time $t_s$. When the clock goes off, the charge of the inversion layer must then be eliminated. This will be discussed in detail in Section 2.5.

2.3 CIRCUIT DESCRIPTION AND OPERATION OF A ONE-BIT SHIFT REGISTER FOR A STANDARD N-CHANNEL SILICON-GATE PROCESS

The circuit schematic of a one-bit shift register is shown in Figure 2.4. The pull-up capacitors are assumed to be varactors, symbolized as shown. The four-phase overlapping clock pulses are shown in Figure 2.5. This is not necessarily the way the device would be used in application, two-phase and three-phase operation being also possible, but it is the simplest for initial characterization.

Since the signal in any one inverter is present only when its clock is ON, another inverter must be ready to accept the signal before the clock goes OFF, i.e. the clock pulses must be overlapping. The series of dotted lines, Figure 2.5, show the progression of a logical input ONE through the bit delay. For $V_{in} > V_T$, we see, during the rise time of $\phi_1$, an initial positive-going spike at the first inverter output, representing the discharging of node $D_1$ to ground, and a negative-going spike associated with $\phi_1$ going off. This latter spike shows the inversion-layer charge under the $C_L$ electrode being injected to ground via the source or the substrate, or both. Since $\phi_2$ comes ON a quarter-period later than $\phi_1$, by which time the gate of the
Figure 2.4. Circuit schematic of a four-phase one-bit shift register.
Figure 2.5. Progression of a high input ($V_{in} > V_T$) logic level through the one-bit delay (dotted lines). The input (top trace) and the four-phase overlapping clock pulses (solid lines) are also shown.

...driver transistor of the second inverter is below threshold, the potential at $D_2$ rises in unison with the clock pulse but reduced by the capacitive divider ratio.

It should be noted that the capacitive voltage divider action for a high output does not begin from ground but begins from whatever floating voltage that remained on $D_2$ due to some previous forward bias of the $D_2$ drain-diffusion to the substrate. The magnitude of
this voltage depends on the frequency of operation as well as the
clock pulse height and the capacitance $C_L$.

The potentials at nodes $D_3$ and $D_4$ are similar to that of $D_1$ and
$D_2$ respectively delayed by one-half period.

2.4 DESIGN OF TWO SHIFT REGISTERS

Figure 2.6 shows a 10-bit shift register realized using a
standard n-channel silicon-gate process. The four clocks and a ground
line are across the top. The signal from the previous bit is passed
from the left to the $\phi_1$ inverter and then around in an inverted U-
shape to the $\phi_4$ inverter. The inverters grow in size from $\phi_1$ to $\phi_4$ to
enable large capacitive loads to be driven from $\phi_4$ in every bit delay,
for example, in a serial-to-parallel shift register application or for
driving an oscilloscope probe for testing. The width of the pull-up
capacitors is 28 $\mu$m. This circuit is designated as the Large-Area
Device.

Figure 2.7 shows 3-bit delays at the output end of a 16-bit
shift register. Ground is at the centre and the signal is passed
alternately back and forth across ground. The pull-up capacitors are
placed under the clock lines giving an area saving. The contact
windows are 6 $\mu$m x 8 $\mu$m. The area per bit delay is less than 20 mils$^2$
including clockline busbars, contact areas and unused areas between
devices. This circuit is designated as the Small-Area Device. To
allow enough capacitive drive off-chip, the last three pull-up inver-
ters are increased in area by about 60% per inverter. The final stage
has provision for either an external pull-up capacitor or a pull-up
resistor.
Figure 2.7. The output end of a 16-bit shift register (Small-Area Device).
Table 2.1 gives some pertinent device characteristics for both the Large-Area and Small-Area Devices.

**Table 2.1. Large-Area and Small-Area Device Parameters.**

<table>
<thead>
<tr>
<th>Large-Area Device</th>
<th>Load Capacitor $C_L$ (pF)</th>
<th>Output Capacitor $C_O$ (pF) at $V_{out} = 0$ V and $V_T = 1$ V</th>
<th>MOST W/L Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter 1</td>
<td>0.9</td>
<td>1.08</td>
<td>11.6</td>
</tr>
<tr>
<td>Inverter 2</td>
<td>1.3</td>
<td>1.76</td>
<td>19.6</td>
</tr>
<tr>
<td>Inverter 3</td>
<td>1.9</td>
<td>3.23</td>
<td>33.0</td>
</tr>
<tr>
<td>Inverter 4</td>
<td>4.2</td>
<td>9.09*</td>
<td>75.6</td>
</tr>
<tr>
<td>Small-Area Device</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>All inverters</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>identical</td>
<td>0.27</td>
<td>0.58</td>
<td>2.5</td>
</tr>
</tbody>
</table>

Excluding Probe Capacitance
Figure 2.8. The top four traces (20V/div) show the overlapping clock pulses $\phi_1$ to $\phi_4$. Bottom trace: output after one-bit delay for an input word of alternate ZERO and ONE (2V/div). Horizontal scale: 0.2 $\mu$s/div.

Figure 2.8 shows a picture of the output waveforms at node $D_4$ for the Large-Area Device with an alternating ONE-ZERO input word. The first four traces show the overlapping 8-volt, 1.25 MHz clocks. The output of the $\phi_4$ inverter, bottom trace, should be looked at in conjunction with the $\phi_4$ clock, fourth trace. The high level output is seen to be in phase with the $\phi_4$ clock. Also seen is the waveform associated with a low logic level output.
2.5 COMPUTER SIMULATION OF A ONE-BIT SHIFT REGISTER

The circuit model of Figure 2.1 was used to simulate the operation of the capacitor pull-up inverter. In this simple model, \( C_L \) was taken equivalent to a discrete capacitor of value \( A \cdot C_{ox} \) where \( A \) is the area of the varactor and \( C_{ox} \) the gate-oxide capacitance per unit area. The threshold voltage was taken into account by assuming that the applied voltage was \( (V_F - V_T) \) rather than \( V_F \). \( C_Q \) included the drain junction capacitance as well as the field-induced junction capacitance under the pull-up electrode. In forward bias, the drain junction capacitance was arbitrarily limited to ten times its value at zero bias. Also, the zero-bias value of the field-induced junction capacitance was assumed equivalent to that of a diffused junction of the same area.

For the case where a back-gate bias \( V_{BS} \) was used, the various capacitive components were adjusted to take this into account. The transistor model is built in the software package developed by Bell-Northern Research [5]. For use in simulation of one bit of the shift register, this basic model has been cascaded four times with appropriate clock voltages applied.

This simple model is intended to show the functional operation of the inverter. The following assumptions and approximations have been made to get at the essential circuit behaviour:

(i) No minority carrier diffusion capacitance (storage) is included.

(ii) Surface conductance under the capacitor \( C_L \) is assumed infinite. Hence the effect of the dynamics of charge flow under the pull-up electrode is neglected.
(iii) No substrate resistance factors have been included.
(iv) Charge-injection effects with respect to the field-induced junction are neglected.

The computer simulation results at the output of the first bit of the Large-Area shift register are shown in Figure 2.9 for an input of alternate ONE's and ZERO's (dashed lines). Also shown are the corresponding experimental results for the Large-Area Device (solid lines). Table 2.2 gives some device and circuit parameters. As far as functional behaviour is concerned, the simulation results are in good agreement with the experimental data obtained. The clocks are 8 V in height at a frequency of 1 MHz. The output signal level is low because of the relatively large capacitive loading on the output due to the oscilloscope probe and package capacitance. Time slots $t_0$, $t_1$, ..., $t_7$, shown in Figure 2.9 represent the times during which changes are occurring in the output signal levels and are associated with the rise and fall times of the various clocks. Figure 2.9(a) shows the results for zero substrate bias while Figure 2.9(b) shows results for -2 V substrate bias.

Table 2.2. Large-Area Device and circuit parameters used in the simulation of the one-bit delay.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold voltage</td>
<td>$V_T$ ($V_{BS}=0$ V) = 0.6V</td>
</tr>
<tr>
<td>Substrate resistivity</td>
<td>$3.5 - 4.5$ ohm-cm</td>
</tr>
<tr>
<td>Clock risetime</td>
<td>3 nS</td>
</tr>
<tr>
<td>Clock falltime</td>
<td>4 nS</td>
</tr>
<tr>
<td>Oscilloscope bandwidth</td>
<td>250 MHz</td>
</tr>
<tr>
<td>Oscilloscope probe capacitance</td>
<td>7 pF</td>
</tr>
</tbody>
</table>
Figure 2.9. Experimental (solid lines) and computer simulation (dashed lines) results for a one-bit delay output with a ONE-ZERO input. Substrate bias (a) $V_{BS}=0$ V. (b) $V_{BS}=-2$ V. Frequency = 1 MHz; $V_F = 8$ V; $V_I = 0.6$ V.
During the rise time of the $\phi_4$ clock, at time slot $t_6$, the drain potential rises to the capacitive voltage divider value from some initial negative potential. At $t_1$ is seen a small capacitive feed-through effect from the previous clock ($\phi_3$ in this case). At $t_2$, in unison with the fall time of the $\phi_4$ clock, the drain potential is returned to a value slightly more negative than the initial value. During the rise time of the $\phi_3$ clock at $t_3$, the high level output of the third inverter turns the MOST of the output inverter ON and its drain is therefore grounded. During the rise time of the $\phi_4$ clock, at $t_4$, the low output level is developed by the grounding action of the source. At $t_5$, the $\phi_3$ clock goes OFF and the output node is left floating at ground or at a slightly negative potential. The $\phi_4$ clock going OFF, at $t_6$, results in a negative-going action from ground.

In Figure 2.9(a), with zero substrate bias, this negative-going action from ground forward biases the drain diffusion and injects charge into the substrate. Such charge, if collected by any reverse-biased diffusion nearby, will degrade a signal that is capacitively stored there. A rather large discrepancy between the experimental and simulation results occurs in time slot $t_6$. This is attributed to the previously quoted approximations.

With a -2 V substrate bias, Figure 2.9(b), the drain-substrate diode is never in forward bias and no substrate injection occurs. The drain diffusion is now the most negative diffusion of the device. Charge from the drain now flows to the grounded source through the conducting channel of the driver MOST in the source-follower mode. This charge flow raises the drain potential until the input MOST turns
itself off due to the source-follower transient*. Thus, the drain diffusion is left floating at a potential equal to one threshold below ground. If this potential was the reference voltage from which a high level output developed, circuit operation would be much degraded because the high level output would not properly rise to the threshold of a following inverter. However, there is an effect, seen at time slot $t_7$, which will raise the drain potential toward ground. During time slot $t_7$, if the next signal to be developed by the inverter output is high, the previous inverter is at this moment developing the spike on its output. This spike raises the potential of the input of the fourth inverter momentarily and allows a significant amount of charge to be injected back to the source. In the limit, the drain diffusion may even be left floating at ground.

2.6 CONCLUSIONS

The theory of operation of the capacitor pull-up inverter was explained as was the operation of a one-bit shift register. The design of the shift registers shows that capacitor pull-up circuitry is easily realizable with MOS processes and the layout of the shift register primitive cell is very simple. The fabrication process was not pushed to its limits in the design of the Small-Area Device. The

* Note that this occurs even if there is no substrate (back-gate bias) effect. However, with no substrate bias, charge is also injected into the substrate, degrading the circuit operation.
contact windows were 6 μm x 8 μm instead of 6 μm x 6 μm while the gate lengths, L, were maintained at the usual length of 8 μm. The design for two-phase and three-phase operation will be different and will be discussed in Chapter 5. Computer simulations showed that theory and experiment were in accord with each other as far as functional behaviour was concerned.

The work described in this Chapter was presented at the 1974 IEEE Electron Devices Conference [6], and published in the October 1975 Special Issue of the Journal of Solid State Circuits [7].
CHAPTER 3

EXPERIMENTAL RESULTS OF 10-BIT AND 16-BIT SHIFT REGISTERS

3.1 INTRODUCTION

The shift registers described in Section 2.4 were designed for a standard n-channel silicon-gate process with a threshold of 1 V. The devices themselves were fabricated at Bell-Northern Research. Substrate resistivities ranging from 1 Ω-cm to 10 Ω-cm, of <100> orientation, were used. Hence, threshold voltages varying from 0.1 V to 1.2 V were obtained allowing a wide range of testing to be carried out. In Section 3.2 are presented some of the experimental results obtained.

3.2 EXPERIMENTAL RESULTS

Figure 3.1(a) shows the experimental peak output levels $V_{p1}$ and $V_{p0}$ as defined in Figure 2.2 versus clock pulse height. The results shown are for Large-Area Devices with a threshold of 0.87 V. The clock frequency is 1 MHz. The output is loaded with a 7 pF probe.

The peak value of the positive-transient spike for a low level output, $V_{p0}$, reaches a maximum as the clock pulse height is increased. This is due to the variation in the transconductance of the MOST with the amplitude of the input signal.

Figure 3.1(b), for the Large-Area Device with a threshold voltage of 0.87 V, shows the measured width of the transient grounding spike, $t_s$, for a low level output as a function of clock pulse height.
Figure 3.1. a) Peak output voltage versus clock pulse height. $V_{p1}$ = peak high logic level, $V_{p0}$ = peak low logic level.
b) Set-up time, $t_s$, for a low-level output versus clock pulse height.
This is essentially the set-up time of the capacitor pull-up inverter, since the output spike must have dropped below threshold before information is passed on. The maximum operating frequency for various clock pulse heights can hence be estimated. For 10 V clocks, for instance, $t_s = 10$ nS and the period, $T$, for four inverters is thus $T = 40$ nS, thus making frequencies of operation of 25 MHz possible. At 2 V clocks, $t_s = 50$ nS, $T = 200$ nS and maximum operating frequency = 5 MHz. It should be noted that these results are valid for the output inverter loaded with a 7 pF probe.

Figure 3.2 shows the minimum clock voltage required for operation of the Large-Area Device versus substrate bias with frequency as parameter and with two different thresholds. The theoretical curves (dashed lines) are plotted on the assumption that the high level of the clocks needs only be 0.5 V greater than the value required to produce an output voltage of $V_T$. The relevant equation is:

$$V_{\text{min}} = \left\{ V_T \left( \frac{C_L + C_0}{C_L} \right) + 0.5 \right\} + V_T$$

The positive slope is due to the substrate bias effect on $V_T$. The experimental and theoretical curves fit well at 1 MHz and below. At higher clock frequencies, because of the effect of the set-up time of the inverter, discussed previously, the circuit requires higher amplitude clocks to operate. The dip in the experimental curve at 20 MHz is ascribed to the effect of charge injection back to source rather than to substrate.
Figure 3.2. Minimum clock voltage required, $V_{\text{min}}$, versus substrate bias voltage, $V_{\text{BS}}$, for Large-Area Devices of two different thresholds. The dashed lines show the theoretical curves.
Figure 3.3 shows the minimum clock voltage required to operate the 16-bit shift register made on a 10 Ω-cm substrate versus substrate bias, with clock frequency as the parameter. Threshold voltage and field threshold voltage were 0.1 and 5.0 V respectively. The dashed line is drawn to pass through the minimum clock pulse height required at each frequency, i.e. the minima of the curves. The device continued to run well at higher values of substrate bias. It can be seen that this circuit ran at 0.4 V clocks at 1 MHz (speed-power product = 0.03 pJ) and 3.2 V clocks at 25 MHz. Further, at higher frequencies, the circuit ran best with a small substrate bias due to the beneficial effects of charge injection back to source rather than to substrate.

Figure 3.4 shows a plot of the measured peak negative drain potential, $V_p$, during the clock pulse fall time, for a low level output on the Large-Area Device with 0.6 V threshold and 8 V clocks. The dashed line shows the boundary for significant substrate injection assuming that a junction diode should be forward biased by 0.6 V for significant injection. At about -1 V substrate bias, injection is practically eliminated.

The output of the Small-Area Device running at 34.5 MHz is shown in Figure 3.5, together with the $\phi_4$ pulse (top trace). The clocks are all 5.5 V, the threshold voltage is 0.1 V, the probe capacitance is 3.5 pF and the substrate bias is -3 V. Figure 5.6 shows the output of both the Large-Area and the Small-Area Devices running at 1 MHz with minimum clock voltages. The top trace shows the Large-Area Device running with 1.2 V clocks ($V_t=0.3$ V) while the bottom trace is for the Small-Area Device running with 0.4 V clocks ($V_t=0.1$ V).
Figure 3.3. Minimum clock voltage required, $V_{\text{min}}$, versus substrate bias voltage, $V_{BS}$, for small-area device with threshold $V_T=0.1$ V. The dashed line represents the minimum operating voltage at each frequency.
Figure 3.4. Graph of the experimental peak negative drain potential, $V_P$, versus substrate bias, $V_{BS}$. Dashed line shows boundary for significant substrate injection.
The high level of the output does not reach threshold only because we are looking at the last stage where the capacitive loading is relatively large due to the scope probe. An external discrete capacitor (5 pF) was used as the pull-up capacitor of the 16-bit register.

In the top trace of Figure 3.6, the action occurring at time slot $t_7$ of Figure 2.9, as discussed in Section 2.5, is evident. Without this action, the high level output would not rise higher than the inverter threshold, particularly for low clock levels.

The performance data presented was taken with the output node loaded rather heavily with an oscilloscope probe, either of 7 or 3.5 pF.
Figure 3.6. Output for minimum clock voltage operation at 1 MHz. Top trace: Large-Area Device, 1.2 V clocks, $V_T = 0.3 \text{ V}$, $V_{BS} = 0 \text{ V}$. Vertical: 0.2 V/div. Horizontal: 0.5 μs/div. Bottom trace: Small-Area Device; 0.4 V clocks, $V_T = 0.1 \text{ V}$, $V_{BS} = 0 \text{ V}$. Vertical: 0.1 V/div.

This loading severely limits the speed capability, i.e. the shift register performance is determined by the loaded output stage, not by the shift register itself. Since the width of the set-up time is essentially the RC time constant of the inverter, the use of an oscilloscope probe increases this time constant and consequently reduces the speed capability of the shift register. For instance, the speed of the output inverters as shown in Figure 3.1(b) is reduced by the ratio $\left(\frac{C_0 + C_{probe}}{C_0}\right)$. Using the data provided in Table 2.1, we note that the RC time constant of the internal inverters is decreased by a factor of 1.8. Hence, the internal inverters are faster.
3.3 CONCLUSIONS

MOS capacitor pull-up circuits, fabricated with a standard n-channel silicon-gate process, have been tested and successfully operated. The direct cascading approach has been shown to increase the operation frequency to about twice the limit of conventional MOS dynamic circuits fabricated with the same silicon-gate process. The degrading effects of charge injection to the substrate, noticeable at higher frequencies, have been eliminated by using a substrate bias, and the capacitor pull-up shift registers have been demonstrated to operate at 34.5 MHz with 5.5 V clocks. This ability to operate at a higher than normal clock rate is possible because the circuit substitutes a single discharge to ground for the normal sequence of a precharge followed by a conditional discharge to ground found in more common MOS dynamic logic circuits.

It should be noted that the frequency of 34.5 MHz quoted was not the limiting frequency of the shift register. However, the word generator available could not operate at higher frequencies and hence the shift registers could not be tested to the limit.

The material presented in this Chapter has been presented in the October 1975 Special Issue on Memories of the Journal of Solid State Circuits [7].
CHAPTER 4

DEVELOPMENT OF AN IMPROVED PROCESS FOR CAPACITOR PULL-UP CIRCUITS

4.1 INTRODUCTION

It has been demonstrated in the previous Chapters that capacitor pull-up circuitry is capable of being operated at frequencies much higher than can be obtained with conventional MOS dynamic logic. Moreover, the use of a standard n-channel silicon-gate process results in a simple structure and relatively low power dissipation. However, the silicon area required for implementation of a bit delay is more than twice that of conventional MOS dynamic logic and, from an LSI point of view, this is unfavourable. Recently, more sophisticated processing [8] has reduced the area required for implementation of both MOS and bipolar circuits. In many cases, the reduction in area is accompanied by higher operating speeds and lower power dissipation per gate. It is with this view in mind that this Chapter presents the development of a new, improved process to improve the implementation and operational characteristics of capacitor pull-up circuitry resulting in higher speeds, lower power dissipation and less area per gate.

Section 4.2 deals with the development and justification of substructures* of a process, required to improve the operational

* Here, substructures refer to integrated circuit elements normally not describable as discrete circuit elements in the usual sense, for example, contacts and interconnects.
characteristics and reduce the power dissipation and silicon area per inverter gate. In Section 4.3 is sketched a process which incorporates such substructures. This is basically a two-level silicon-gate process, employing the use of five photolithographic steps. This process overcomes the gross disadvantage inherent in using the standard single-level silicon-gate process for capacitor pull-up circuitry. Deviations from the processing procedure due to limitations of available equipment are discussed in Section 4.4, while conclusions are made in Section 4.5.

4.2 DISCUSSION OF PROCESS SUBSTRUCTURES FOR IMPROVED CIRCUIT PERFORMANCE

4.2.1 Introduction

In this Section will be discussed process substructures that have not been extensively reported in the literature regarding a standard two-level polysilicon-gate process, such as the process described in Reference 9. The substructures include a linear capacitor with polysilicon electrodes on top of the field oxide, and polysilicon-to-silicon (buried) contacts. Besides serving as a contact to silicon, the polysilicon in the latter substructure also acts as a diffusion source and as a second interconnection level. These two substructures will be described in Subsection 4.2.2, while the rationale for having these substructures is presented in Subsection 4.2.3.
4.2.2 Description of Substructures

In Figure 4.1 are shown integrated structures of pull-up capacitors and associated circuit schematics. The structure shown in Figure 4.1(a) is a metal-on-diffusion capacitor. The top electrode is aluminum while the N⁺ diffusion (for an N-channel process) serves as the bottom electrode. The circuit model representing the capacitances associated with this structure are also shown. \( C_L \) represents the oxide capacitance while \( C_j \) represents the parasitic diffusion junction capacitance. In addition to the parasitic capacitance, \( C_j \), it is assumed that there is some arbitrary loading capacitance, in parallel with \( C_j \), and in addition to it. This is true for all cases shown in Figure 4.1. At a potential of 0 volts, the value of \( C_j \) is approximately the same as the value of \( C_L \). As \( V_{out} \) increases positively, for n-channel, the value of \( C_j \) is reduced. For a clock pulse height \( V_\phi \), the output voltage is:

\[
V_{out} = \left( \frac{C_L}{C_L + C_j} \right) V_\phi
\]

This value is true for all values of the threshold voltage, \( V_T \), of the device.

The structure shown in Figure 4.1(b) is a polysilicon-oxide-silicon pull-up capacitor (varactor), where the top electrode of \( C_L \) is formed at the same time as the gate electrode of the MOST. The bottom electrode is only formed after the clock \( V_\phi \), reaches a value \( V_\phi = V_T \).

\* This assumes that the surface inverts at \( V_\phi = V_T \). The case of weak inversion is neglected.
Figure 4.1. Integrated structures of pull-up capacitors and associated circuit schematics for (a) the metal-gate process, (b) the single-level silicon-gate process, (c) the modified double-level silicon-gate process.
and an inversion layer exists at the surface. This inversion layer acts as the bottom electrode of $C_L$ and joins this electrode to the adjacent $N^+$ diffusion. The parasitic capacitance of this field induced junction, $C_{FINV}$, is in series with $C_L$ and is equal to about $(2/3)C_L$ at the onset of strong inversion and decreases in value as the potential of the $N^+$ diffusion increases positively. The output voltage, $V_{\text{out}}$, for a clock voltage height $V_\Phi$ is therefore:

$$V_{\text{out}} = \left( \frac{C_L}{C_L + C_{FINV}} \right) (V_\Phi - V_T)$$

In Figure 4.1(c) is shown a polysilicon-to-polysilicon linear capacitor on top of the field oxide. This structure is available in the double-level polysilicon-gate process that will be presented in Section 4.3 and is the first substructure that will be described. Both electrodes are here formed of polysilicon with the oxide dielectric thermally grown on the bottom electrode. This latter electrode lies on top of the field oxide and forms a parasitic field oxide capacitance, $C_{FO}$, between it and the silicon surface, in series with $C_L$. For n-channel enhancement-mode devices, there is an additional depletion capacitance, $C_D$, between the silicon surface below $C_L$ and the bulk substrate. The total capacitance in series with $C_L$ is $(C_{FO}C_D)/(C_{FO} + C_D)$ and is always less than $C_{FO}$, which is primarily dependent on the field oxide thickness. It is seen that $C_{FO}$ can be made very small indeed by increasing the field oxide thickness. For an applied clock pulse height, $V_\Phi$, the value of $V_{\text{out}}$ is:
\[ V_{out} = \left[ \frac{C_L}{C_{FO}C_D} \right] \left[ \frac{C_{FO}C_D}{C_L + \frac{C_{FO}C_D}{C_{FO} + C_D}} \right] V_\phi \]

In Figure 4.1(c), the bottom polysilicon electrode of \( C_L \) extends over the field oxide step into the diffusion well. Here, the polysilicon makes contact to the silicon substrate avoiding the necessity of metal contacts to the diffusion and to the polysilicon itself. The polysilicon also acts as a diffusion source for the \( N^+ \) diffusion and serves as an interconnection track below the top polysilicon level and the metal. This is the second substructure that is available in the process presented in Section 4.3. It should be noted that the silicon surface below the lower electrode of the load capacitor, \( C_L \), cannot be inverted since the diffusion is physically linked to this electrode. This prevents the surface from reaching inversion, assuming enhancement mode devices, and hence \( C_D \) remains a depletion capacitance.

The reasons for incorporating the two substructures just described in a capacitor pull-up process are discussed in the next subsection.

4.2.3 Rationale for Substructures

a) Linear capacitor on top of field oxide

As has been explained in Chapter 2, the peak value of the high output voltage level, \( V_{P1} \), is dependent on the clock voltage height, \( V_\phi \), and the capacitive divider ratio \( \frac{C_L}{(C_L + C_D)} \). As in Figure 4.1(b),
for the standard silicon-gate process, where the pull-up capacitor is achieved functionally through the use of a varactor, and the silicon surface has to be inverted for successful operation, then

\[ V_{pl} = \left( \frac{C_L}{C_L + C_O} \right) (V_\phi - V_T) \]

Hence, the effective voltage that is capacitively divided is \((V_\phi - V_T)\) rather than \(V_\phi\). Here, \(C_O\) is the total output capacitance, including the parasitic capacitance \(C_{FINV}\), Figure 4.1(b).

For the metal-gate process, Figure 4.1(a), the peak output voltage level, \(V_{pl}\), is:

\[ V_{pl} = \left( \frac{C_L}{C_L + C_O} \right) V_\phi \]

The voltage that is capacitively divided is \(V_\phi\) and not \((V_\phi - V_T)\) since the capacitor is a metal-on-diffusion capacitor, with the diffusion electrode being an extension of the drain diffusion.

For equal values of \(C_L\) and \(C_O\) in the metal-gate and in the standard silicon-gate process, the peak output level is larger in the metal-gate. To achieve the same value of inverter output \(V_{pl}\) in the silicon-gate process as in the metal-gate process, it is necessary to increase the value of the capacitor \(C_L\) or the height of the clock voltage, \(V_\phi\). Both approaches are undesirable since the former increases the size of the device while larger clock voltages increase the power dissipation. Furthermore, it has been shown that a substrate bias is greatly beneficial for the successful operation of the devices.
at high frequencies. Under such conditions, the effective threshold voltage is increased, especially for n-channel devices, and the driving voltage, $V_T - V_T$, is consequently reduced. The effect of $V_T$ on the value of $V_{pl}$ can be minimized by using low threshold voltage devices (e.g. 0.1 V). Here the noise margin is very low and the reliability of operation is decreased.

Use of the polysilicon-to-polysilicon capacitor, shown in Figure 4.1(c), removes the threshold voltage effect on $V_{pl}$ and reduces the parasitic capacitance in series with $C_L$. The former is achieved because the capacitor $C_1$ is a linear capacitor independent of the device threshold, $V_T$, or changes in $V_T$ due to applied substrate bias. The parasitic capacitance is reduced because the depletion capacitance, $C_D$, is in series with $C_{FO}$, the field oxide capacitance. The value of $C_{FO}$ can be chosen to suit a particular circuit requirement by increasing or decreasing the field oxide thickness and can be made very small. Since the parasitic capacitance forms part of $C_O$ and is decreased, then for the structure of Figure 4.1(c), the capacitor divider ratio, $(C_L/(C_L+C_O))$, is correspondingly increased, resulting in an optimum value for the high output voltage level, $V_{pl}$.

Table 4.1 presents assumed process parameters for the capacitance structures shown in Figure 4.1. For a load capacitor area of 20 µm x 20 µm and a field oxide thickness of 0.5 µm, the relevant

* In Figure 3.3 of Chapter 3, it was shown that a substrate bias was essential to operate the standard n-channel silicon-gate 16-bit shift register (Small-Area Device) at frequencies greater than 25 MHz.
Table 4.1. Calculation of capacitance values for the structures of Figure 4.1.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>VALUE</th>
<th>UNIT</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{ox}$</td>
<td>$3 \times 10^{-4}$</td>
<td>pF/μm$^2$</td>
<td>Gate oxide capacitance per unit area</td>
</tr>
<tr>
<td>$C_{jA}$</td>
<td>$1.1 \times 10^{-4}$</td>
<td>pF/μm$^2$</td>
<td>Diffusion junction capacitance per unit area, at 0 V</td>
</tr>
<tr>
<td>$C_{jP}$</td>
<td>$5.5 \times 10^{-4}$</td>
<td>pF/μm</td>
<td>Peripheral diffusion junction capacitance, at 0 V</td>
</tr>
<tr>
<td>$C_L$</td>
<td>0.12</td>
<td>pF</td>
<td>Area of $C_L = 20 \mu m \times 20 \mu m$</td>
</tr>
<tr>
<td>$C_j$</td>
<td>0.079</td>
<td>pF</td>
<td>Parasitic diffusion junction capacitance, at 0 V</td>
</tr>
<tr>
<td>$C_{FINV}$</td>
<td>0.044</td>
<td>pF</td>
<td>Parasitic field induced junction capacitance, at $V=V_T$</td>
</tr>
<tr>
<td>$C_{FO}$</td>
<td>0.026</td>
<td>pF</td>
<td>Parasitic field oxide capacitance; field oxide thickness = 0.5 μm</td>
</tr>
<tr>
<td>$C_D$</td>
<td>0.49</td>
<td>pF</td>
<td>Parasitic depletion capacitance, at 0 V</td>
</tr>
<tr>
<td>$\frac{C_L}{C_L + C_j}$</td>
<td>0.60</td>
<td></td>
<td>Capacitive divider ratio for metal-gate pull-up capacitive structure at 0 V</td>
</tr>
<tr>
<td>$\frac{C_L}{C_L + C_{FINV}}$</td>
<td>0.73</td>
<td></td>
<td>Capacitive divider ratio for silicon-gate pull-up capacitive structure at $V=V_T$</td>
</tr>
<tr>
<td>$\frac{C_L + \frac{C_{FO}C_D}{C_{FO} + C_D}}{C_L + \frac{C_{FO}C_D}{C_{FO} + C_D}}$</td>
<td>0.83</td>
<td></td>
<td>Capacitive divider ratio for two-level polysilicon-gate pull-up capacitor at $V=0$ V</td>
</tr>
</tbody>
</table>
capacitance values are calculated. The improvement obtained by using the polysilicon-to-polysilicon capacitor is evident.

b) The polysilicon-to-silicon (buried) contact

The disadvantages of using metal contacts and the advantages of using polysilicon (buried) contacts are now described.

Consider the schematic diagram of two cascaded capacitor pull-up inverters using the single-level polysilicon-gate process which is shown in Figure 4.2. This was the layout used to design the Small-Area Device of Chapter 2. All the tolerances used here are the minimum allowable in the standard n-channel silicon-gate process available at Bell-Northern Research. It is noted that the minimum MOST drain area is dictated by the minimum metal-to-silicon contact area required. Because the area of the MOST drain diffusion is large, the associated junction capacitance is large. This increases the value of the inverter output capacitance, \(C_O\), and the value of the set-up time \(t_s\), while it reduces the capacitor pull-up ratio, \(\frac{C_L}{C_L+C_O}\). It is therefore essential to reduce the drain junction capacitance to a minimum.

Also shown in Figure 4.2 is the area wastage between inverters due to the necessity of having metal contacts to the MOST gates on top of the field oxide rather than on top of the gate oxide itself.

The main advantages of using the polysilicon-to-silicon contact shown in Figure 4.1(c) are:

i) a reduction in the area of the MOST drain and source diffusions and its corresponding drain junction capacitance and;
Figure 4.2. Schematic of two cascaded capacitor pull-up inverters using the single-level polysilicon-gate process.
ii) a reduction in the area wasted on the field-oxide due to metal-to-polysilicon contacts.

In Figure 4.3 are shown schematics of minimum area transistor structures for (a) the metal-gate process, (b) the standard silicon-gate process and (c) a two-level silicon-gate process employing buried contacts. Figure 4.3(c) shows topographically how the polysilicon contacts to source and drain described in Figure 4.1(c) are achieved. For a contact area of 6 μm x 6 μm shown cross-hatched in Figures 4.3 (a) and (b) and mask-to-mask tolerances of 4 μm, the minimum area required is 14 μm x 14 μm. It is also necessary to leave a metal-to-metal or a metal-to-polysilicon spacing, as shown in Figure 4.3. This increases the size of the transistor further.

Figure 4.3(c) shows how the area of the drain diffusion is reduced by using polysilicon contacts. The resulting reduction in junction capacitance reduces the value of the output capacitance, $C_O$, and increases the value of the capacitive divider ratio, $\left[\frac{C_L}{C_L + C_O}\right]$. The peak output voltage level, $V_{pl}$, is correspondingly improved.

Since the polysilicon forming the contact to the diffusions and the polysilicon-gate are etched at the same time, the contacts and gates are self-aligned with respect to each other resulting in smaller transistor areas without loss of reliability. Further, since the polysilicon contact can be extended, from the diffusion to the gate, any electrical connection between diffusions and transistor gates may be achieved without the need for metal contacts on top of the field oxide. This reduces the area wastage between the inverters.
Figure 4.3. Schematics of minimum area transistor structures for (a) the metal-gate process, (b) the standard silicon-gate process, (c) a polysilicon process with buried contacts.
Table 4.2 gives relevant information about the minimum-area transistor structures of Figure 4.3 using the same process parameters as assumed in Table 4.1. The information provided shows that transistor and junction sizes are reduced by a factor of 2 or 3, as are junction capacitances.

4.3 **SKETCH OF A TWO-LEVEL POLYSILICON-GATE PROCESS**

Figure 4.4 shows a sequence of a five photomask, two level, n-channel silicon-gate process. This process is meant to incorporate the substructures described in the previous Section. All design rules and processing parameters are the same as for the standard silicon-gate process which was used in the fabrication of the shift registers discussed previously. The typical processing steps are as follows:

Step A: A P-type silicon slice, <100> orientation, with a resistivity typically of 1 Ω-cm to 3 Ω-cm is pre-furnace cleaned. A 0.5 μm thick field oxide is grown at 1150°C. A thin phosphorus doped polysilicon layer of thickness 0.26 μm is deposited in an epitaxial reactor followed by a low temperature (400°C) silox deposition of thickness 0.2 μm. This oxide is densified in a furnace at 900°C for 10 minutes.

Step B: Photomasking Step #1. The device well is opened by the successive etching of oxide, polysilicon and oxide. All the oxide on top of the first polysilicon layer hereafter called Poly 0, is removed during the second oxide etch. The first polysilicon layer is termed 'Poly 0' because it lies below the polysilicon layer of the
Table 4.2. Comparative information for minimum area MOS transistor structures in the metal-gate, standard silicon-gate and a two-level polysilicon gate process.

<table>
<thead>
<tr>
<th>DEVICE ELEMENTS AND GEOMETRIES</th>
<th>UNITS</th>
<th>METAL-GATE PROCESS</th>
<th>STANDARD SILICON-GATE PROCESS</th>
<th>TWO-LEVEL SILICON-GATE PROCESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOST Device Well Area</td>
<td>μm²</td>
<td>756</td>
<td>588</td>
<td>250</td>
</tr>
<tr>
<td>Area of Drain Diffusion</td>
<td>μm²</td>
<td>364</td>
<td>252</td>
<td>96</td>
</tr>
<tr>
<td>Drain Diffusion Capacitance, at 0 V</td>
<td>pF</td>
<td>0.076</td>
<td>0.055</td>
<td>0.028</td>
</tr>
<tr>
<td>MOST Gate Oxide Capacitance</td>
<td>pF</td>
<td>0.034</td>
<td>0.034</td>
<td>0.019</td>
</tr>
<tr>
<td>Contact Window Area</td>
<td>μm²</td>
<td>36</td>
<td>36</td>
<td>48</td>
</tr>
<tr>
<td>MOST Aspect Ratio, W/L, for junction depth</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>= 1.1 μm</td>
<td></td>
<td>1.75</td>
<td>1.75</td>
<td>1.00</td>
</tr>
</tbody>
</table>

standard single-level silicon-gate process, commonly termed 'Poly 1'.

Step C: A thin gate oxide is grown at 1050° C, of thickness 0.1 μm. The second photolithographic step is performed, opening up contact windows in the source and drain areas and leaving oxide only in the gate region and in the region where the constant capacitor on the field oxide is required.

Step D: A 0.7 μm thick phosphorus doped polysilicon layer is deposited at 650° C. This low temperature is necessary here because it eliminates the formation of whisker growth [10]. This second polysilicon layer, called Poly 1, forms the gate electrode (region X₃).
Figure 4.4. Sequence of a five-photomask, n-channel two-level silicon self-aligned gate process. (continued)
Figure 4.4. Sequence of a five-photomask, n-channel, two-level silicon self-aligned gate process. (Continued from previous page)
the top electrode of the capacitor (region X₆), buried contacts to the substrate (regions X₂ and X₄), and contacts to the Poly 0 layer (regions X₁, X₅, X₇).

Step E: A phosphorus diffusion is performed forming a 2 μm junction beneath the buried contact. During the drive-in part of the diffusion, a 0.1 μm wet oxide is grown.

Step F: The third photomasking step is performed followed by an oxide etch, a polysilicon etch and another oxide etch. The polysilicon is here completely defined, as shown in Figure 4.4, with both the gate and the silicon contact self-aligned with respect to each other.

Step G: Here, a 1 μm deep phosphorus junction is formed linking the former junctions to the gate. Slightly deeper junctions result beneath the contact.

Step H: A 0.7 μm thick silox layer is deposited followed by a thin (250 Å) phosphosilicate silox deposition for MOST stabilization. The fourth photolithographic step is performed opening up contact windows for metal-to-Poly 1 contacts.

Step I: Aluminum metal is evaporated in the usual fashion and a fifth photolithographic step is required to delineate the necessary patterns. Gold is evaporated on the back of the slice for contacts. Both aluminum and gold are annealed in the usual manner. A layer of pyrox may be deposited and a further sixth mask may be used for pad-
window opening.

The process just described shows that:

i) the varactor in the standard Si-gate process can be replaced by a Poly 1 - SiO₂ - Poly 0 capacitor, and a layer of Poly 0 is substituted for the inverted surface of the Si substrate as the lower electrode of \( C_L \);

ii) no metal contacts are required between the Poly 0 - electrode, the drain diffusion and the Poly 1 gate of the driver MOST of the following inverter;

iii) all drain contacts, MOST gates, Poly 1 - SiO₂ - Poly 0 capacitors are self-aligned with respect to each other;

iv) metal clock lines running on thick silane oxide deposited over Poly 1 can contact the electrode directly over the thin oxide. No threshold voltage variations can occur due to this contact as would happen in the standard process.

v) any problems due to metal being in the immediate vicinity of the MOST gates, such as the effects due to the solubility of silicon in aluminum, may be totally eliminated.

4.4 **DEVIATIONS FROM THE PROCESSING PROCEDURE DESCRIBED IN SECTION 4.3**

In discussing the process of Section 4.3, it was assumed that all necessary equipment would be available as in an industrial environment. In the laboratory environment at Carleton, due to the lack of an epitaxial reactor and a silox reactor, different processing procedures had to be used than what is considered as standard. The consequences of these changes are now discussed.
In the absence of an epitaxial reactor, polysilicon was obtained by annealing amorphous silicon that had been electron-beam evaporated in a high-vacuum chamber. This technique has been previously reported [11-17]. Typical information on the evaporation of amorphous silicon that was used in the Carleton facilities is given in Table 4.3.

The main disadvantage of this technique is that local hot spots occur in the silicon melt during evaporation, and small chunks of silicon are ejected forming 'bumps' on the surface [18]. These 'spits', as they are commonly called, make photomasking very difficult because the silicon slice is not able to come into intimate contact with the photomask emulsion everywhere [18]. This reduces the quality of photoresist delineation, most especially near surface steps. Another disadvantage is that these spits tend to scratch the photomask emulsion during alignment. The situation can be improved by using an electron gun whose beam is capable of being rapidly moved across the silicon source so that more even heating is accomplished. Nevertheless, though in this way spits may be reduced, they cannot be avoided altogether. Note that this does not happen during the evaporation of aluminum.

Table 4.3. Information on amorphous silicon evaporation.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Starting Pressure</td>
<td>$2 \times 10^{-8}$ Torr</td>
</tr>
<tr>
<td>Substrate Temperature</td>
<td>$145\pm5$ °C</td>
</tr>
<tr>
<td>Partial Pressure of $H_2O$</td>
<td>$3\times10^{-10}$ Torr</td>
</tr>
<tr>
<td>Pressure during Evaporation</td>
<td>$2\times10^{-7}$ to $3\times10^{-7}$ Torr</td>
</tr>
<tr>
<td>Electron Beam Current</td>
<td>195 to 200 mA</td>
</tr>
<tr>
<td>Evaporation Rate of Amorphous Si Per Minute</td>
<td>$0.058 \mu$m to $0.059 \mu$m</td>
</tr>
</tbody>
</table>
because the metal is a good heat conductor and hence it is easy to maintain the source at constant temperature. Another disadvantage is that when the amorphous silicon is annealed 'blow-outs' occur. Blow-outs are local regions where the amorphous silicon layer undergoes large enough stress during annealing so that chunks of silicon are blown away from the surface leaving empty holes or voids [16]. Figure 4.5(a) shows a typical blow-out while Figure 4.5(b) shows a typical spit.

Another major problem has to do with the size of the crystallites after the amorphous silicon is annealed, since large grain size interferes with the polysilicon edge definition [15]. The grain size obtained is dependent on the annealing temperature and the thickness of the silicon layer [14-16,19], but is only slightly dependent on the ambient atmosphere [19]. A number of trial runs were made in which electron-beam evaporated amorphous silicon layers were annealed in the temperature range 800 °C to 1150 °C, in temperature steps of 50 °C. A photolithographic step, followed by an oxide etch and a polysilicon etch, was done to find the highest temperature at which the grain size was not large enough to interfere with the polysilicon edge definition. It was found that the higher the temperature the larger the crystallite size and that 900 °C was the highest possible temperature at which the resulting polysilicon could be annealed for satisfactory edge delineation. Hence, all diffusions and the gate oxidation had to be performed at 900 °C. The resulting gate oxide is of poorer quality since surface state charge density is much higher [20,21], and
Figure 4.5.  (a) A 'blow-out' or 'void', i.e. a region where the polysilicon has been removed by stresses due to heating.
(b) Silicon 'spits', i.e. chunks of silicon that were blown onto the substrate from the silicon melt due to local hot spots in the melt.
the oxidation and diffusion times are prohibitive. Figure 4.6(a) shows the large polysilicon remnants after a polysilicon etch was performed. These remnants give an idea of the large crystallite sizes after annealing at 1150 °C. Figure 4.6(b) and (c) show the polysilicon edge definition after amorphous silicon was annealed at 1000 °C and at 900 °C respectively. Moreover, since the crystallite size is dependent on the thickness of the silicon layer, (the thicker the silicon layer, the larger was the crystallite size), the etch rates of Poly 1 and Poly 0 were different, all other conditions remaining the same.

When polysilicon is deposited in an epitaxial reactor, it is customary to etch off a thin layer (a few angstroms) off the oxide surface by a gaseous HCl etch [22]. This increases the adherence properties of the polysilicon to the oxide. The same is done when an epitaxial deposition is performed [23]. This etch removes the oxide monolayer that is always present when a surface is exposed to the atmosphere and it also removes a few angstroms off the silicon surface, hence presenting a very clean and fresh surface to the silicon being deposited, resulting in a very good contact [23]. The same treatment should be given to the surface when buried contacts are used, but this is not available when silicon is evaporated in a vacuum chamber. If this is not done, a high contact resistance is present and the thin oxide layer below the silicon contact will mask against phosphorus diffusion.

Another problem that was encountered was due to the unavailability of a silox reactor. Instead of a silox deposition, spin-on oxide was used, and this has two gross disadvantages. When a silicon
Figure 4.6.  (a) Polysilicon remnants are shown after a polysilicon etch was performed to remove all the silicon off the field oxide, (Mag: 500X; annealing temperature, 1150 °C). These remnants are an example of the large polysilicon crystallite size.

(b) A polysilicon sheet resistivity pattern showing rough edge-delineation for an annealing temperature of 1000 °C.

(c) Polysilicon edge-definition for an annealing temperature of 900 °C.
slice is coated with liquid oxide and spun, an oxide build-up occurs at the edge of the slice as shown in Figure 4.7(a). This build-up increases with each successive run, and causes grave photolithographic problems. After coating, the slice is spun at 3000 r.p.m. and a 1 hour heat treatment at 400 °C in dry N₂ is performed between each coating [24]. A final heat treatment at 900 °C is performed after the final coating for densification purposes [24]. Increasing the spin-speed could reduce the build-up but it also results in decreased oxide thickness per coating, necessitating more layers [24,25].

The second problem arises due to the fact that, towards the end of a process fabrication run, the silicon surface is not flat but consists of hills and valleys with many sharp steps. During spinning, these sharp corners act as disturbance centres for the liquid oxide and the resulting oxide is very uneven around these corners because of flow patterns caused by the disturbance centres. After spinning, it is found that oxide ridges are formed with a corner or step acting as the apex. With heat treatment at 900 °C for densification, these apexes often result in cracks, wherever the oxide is most thick. The unevenness also creates problems during photolithography for the same reasons discussed previously. Figure 4.7(b) shows the cracks that develop due to the densification of uneven thickness of the spin-on oxide layer.
Figure 4.7. (a) The diagram shows the build-up of oxide at the edges of the silicon substrate after the spinning operation is completed. (b) The photograph shows the effect of corners and steps on spin-on oxide. The dark splinter-like lines are cracks in the oxide after densification at 900 °C.
4.5 CONCLUSIONS

Particular disadvantages of using the metal gate or the standard silicon gate processes for capacitor pull-up circuits have been discussed. Process substructures have been put forward which, when incorporated in a two-level polysilicon process, could improve the performance of this circuitry, and reduce the area required for its implementation. Such a process was sketched and the procedural steps were briefly outlined. Excepting for the buried contact and the poly-silicon-to-polysilicon capacitor, all other structures, design rules and processing parameters are standard. Deviations from this procedure due to the limitations of the available machinery were discussed.
CHAPTER 5

CIRCUIT AND PROCESSING RESULTS OF THE MORE OPTIMUM PROCESS

5.1 INTRODUCTION

The main aim of this Chapter is to simulate the behaviour of logic circuits that can be fabricated with the fully developed process of Chapter 4. To allow this characterization to be performed, a set of masks was developed, as a design exercise, to obtain relevant areas, geometries and other parameters for use in the computer simulation of the modified circuits. Artwork for a 90 x 90 mil² chip was done, patterns were cut out on rubylith and a set of five photolithographic masks was obtained by standard reduction techniques. The design contained discrete elements such as diodes, capacitors, MOSTs and sheet resistivity patterns as well as three shift registers of several bit delays each. The discrete devices were intended for the initial characterization of a two-level polysilicon gate process which would subsequently be available in the Carleton laboratories. Among these test devices were included polysilicon-to-polysilicon capacitors as well as diodes formed by diffusion through polysilicon into the substrate. These devices were of particular interest because of the lack of material in the literature about them and because, as explained previously, they constitute the main differences between the process described in Chapter 4 and a standard two-level polysilicon-gate process.

These discrete devices were successfully fabricated and tested. Experimental and theoretical results obtained on these substructures
are presented in Section 5.2. In Section 5.3 is discussed the design and simulation of an improved 4-Φ shift register. The theory of operation and simulation results of a three-phase shift register are given in Section 5.4. Section 5.5 deals with the design, operation, simulation and experimental results of a 2-Φ shift register. A comparison between these shift registers and the earlier Small-Area Device, discussed in Chapter 2, is given in Section 5.6, while Section 5.7 concludes the Chapter.

5.2 THEORETICAL AND EXPERIMENTAL RESULTS OF SUBSTRUCTURES

5.2.1 The Linear Polysilicon-to-Polysilicon Capacitor

The structure used for characterization of the polysilicon-to-polysilicon capacitor is shown in Figure 5.1. The bottom electrode, Poly 0, is separated from the substrate by the field oxide, while the top electrode, Poly 1, is separated from the metal pads by a thick layer of SiO₂. Metal contacts to both electrodes are made in the usual fashion. Table 5.1 gives the pertinent data relating to the substructure shown in Figure 5.1.

Experimental results obtained by measurement of the small-signal capacitance are given in Figure 5.2. The small-signal capacitance was measured with a Boonton Electronics, Direct Capacitance Bridge (Model 75D, Test Frequency 1 MHz). The readings are accurate

* The Small-Area Device refers to the 16-bit shift register designed with the standard n-channel silicon-gate process.
Figure 5.1. Cross-section of the polysilicon-to-polysilicon linear capacitor.

Table 5.1. Pertinent data relating to the linear capacitor structure shown in Figure 5.1.

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SiO₂ layer: densified spin-on oxide</td>
<td>0.7 μm thick</td>
</tr>
<tr>
<td>2</td>
<td>Poly 1 layer: vacuum deposited amorphous silicon annealed at 900 °C</td>
<td>sheet resistivity &lt;10 Ω/□ 0.6 μm thick</td>
</tr>
<tr>
<td>3</td>
<td>SiO₂ layer: thermally grown at 900 °C</td>
<td>850 Å thick</td>
</tr>
<tr>
<td>4</td>
<td>Poly 0 layer: vacuum deposited amorphous silicon annealed at 900 °C</td>
<td>sheet resistivity &lt;15 Ω/□ 2000 Å thick</td>
</tr>
<tr>
<td>5</td>
<td>Field oxide layer: thermally grown at 1150 °C</td>
<td>0.5 μm thick</td>
</tr>
<tr>
<td>6</td>
<td>Area of Poly 1 capacitor electrode</td>
<td>200 x 200 μm²</td>
</tr>
</tbody>
</table>
Figure 5.2. Experimental and theoretical results of linear capacitance substructure. [Assumed value of $\varepsilon_{ox} = 3.75$]

to within 0.1%. Also shown are the theoretical results that would be obtained if the polysilicon electrodes were replaced by metallic ones. It is seen that there is a variation of about 0.7% between the theoretical and the experimental curve for positively applied dc bias, which is the region of most interest for n-channel enhancement devices. For negative bias, the variation is much greater, approximately 4.5% less than the theoretically calculated value. The relative permittivity, $\varepsilon_{ox}$, of the SiO$_2$ was assumed to be 3.75. An attempt is now made to
explain these variations.

Figure 5.3(a) shows a symmetrical capacitor structure where an oxide is sandwiched between two heavily doped \( (>10^{20} \text{ cm}^{-3}) \) single crystalline silicon electrodes. If the doping concentration is identical in both electrodes, Figure 5.3(b), then the expected C-V relation is as shown in Figure 5.3(c). For no dc bias voltage applied across the electrodes, the differential capacitance measured is the oxide capacitance, \( C = \varepsilon_{0} A C_{ox} \), where \( C_{ox} \) is the oxide capacitance per unit area and \( A \) is the area. For an applied positive voltage between electrodes 1 and 2 with electrode 2 grounded, a depletion region appears in the silicon of electrode 1 at the Si-SiO\(_2\) interface, while an accumulation region appears at the surface of 2. The resulting depletion capacitance appears in series with \( C \) and the total capacitance is reduced. If the silicon is very heavily doped, this depletion capacitance is very large and only small variations in the total capacitance are noticed with applied voltage. Since the device is assumed completely symmetrical, the curve shown in Figure 5.3(c) results.

The linear capacitor structure that can be achieved by the modified process as described in Chapter 4 is not ideal like that shown in Figure 5.3(a). The electrodes are formed by the deposition of polycrystalline silicon on top of oxide layers and the capacitor dielectric is an oxide that is thermally grown out of the Poly 0 electrode. Because of the passivating properties of a thermally grown oxide, it is assumed that the Poly 0 surface is very similar to that of a single crystalline silicon, on which an oxide is thermally grown. Grain boundaries still separate the crystallites at the Poly 0 - SiO\(_2\) inter-
Figure 5.3. (a) Structure of the Si-SiO₂-Si capacitor. 
(b) Doping concentration versus electrode distance for symmetrical structures. 
(c) Expected C-V curve for structure in (a) 
$C_0 =$ oxide capacitance, $C_{D1}, C_{D2} =$ depletion capacitances in electrodes 1 and 2 respectively.
face but no grain boundaries exist between the crystallites' surface and the oxide. This case is shown in Figure 5.4(a). Also shown is the doping concentration during oxide growth, where \( N_{D0} \) is the original concentration in the polysilicon electrode, and has been assumed to be constant throughout the electrode thickness. A phosphorous build-up appears at the surface because the phosphorous rejection ratio is in favour of silicon. This build-up is less marked than it would be in single-crystal silicon, since the diffusion coefficient of phosphorous in polysilicon is between 10 times to 1000 times faster than in single-crystalline silicon [26-28] resulting in a concentration increase in the bulk, \( N_{D1} \), Figure 5.4(b). Moreover, since the Poly 0 electrode is thin (\( \sim 2000 \) Å) and since more high-temperature steps follow the oxidation, it is assumed that at the end of the processing, redistribution from the case of Figure 5.4(b) occurs, and the Poly 0 layer is nearly uniformly doped at \( N_{D2} \), as shown in Figure 5.4(c).

The polysilicon layer which forms the other electrode is deposited on the thermally grown oxide. The interface between this Poly 1 layer and the oxide is therefore expected to be drastically different from the Poly 0 - oxide interface. This surface condition results in two properties that make the top electrode resemble a metallic electrode as far as the capacitor is concerned. These properties are the result of the grain boundaries that exist at the surface. When a phosphorous diffusion is performed, the concentration of diffusant species in the grain boundaries is much higher than in the crystallites [27-31]. This results in a narrow region of very high phosphorous concentration right at the interface. This region also contributes to
Figure 5.4. (a) Initial oxide growth on Poly 0 layer eliminates grain boundaries at SiO₂-Poly 0 interface. A slight phosphorous build-up, due to impurity redistribution, occurs at the Poly 0 surface. \( N_{D0} \) = original phosphorous concentration in Poly 0.

(b) At the end of the oxidation cycle, the bulk concentration increases from \( N_{D0} \) to \( N_{D1} \). A large phosphorous build-up is at the surface of the Poly 0 layer.

(c) After all high temperature processing is finished, the bulk doping of the Poly 0 layer increases to \( N_{D2} \) and is constant throughout the Poly 0 electrode.
a very high value of interface states. The other property is due to the 'roughness' of the Si-SiO₂ interface, so that a larger number of electronic states are available than for an oxide-passivated surface. Hence, for an applied field, a large number of charges can be accommodated right at the interface and the field penetration in the polysilicon is low, as is the case in a metallic conductor. Under these conditions, the Poly 1 - SiO₂ interface resembles a metal-oxide interface in the usual sense.

For the linear polysilicon-to-polysilicon capacitor structure shown in Figure 5.1, and the data given in Table 5.1, normalized, experimental C-V curves are given in Figure 5.5. For the results shown in this Figure, the Poly 0 electrode was grounded and the voltage on the Poly 1 electrode varied. Negligible shifts in the C-V curves were noted after the capacitors were stressed at +20 V and -20 V followed by a 20 minute heat treatment at 280 °C. When the potentials of the Poly 1 and Poly 0 electrodes were interchanged, no change in the C-V curves was noted. In all cases, the potential of the silicon substrate was kept at the same potential as the Poly 0 electrode. The experimental results obtained were normalized with respect to the largest capacitance value measured, i.e. the capacitance at +20 V. Beyond this voltage, negligible change was perceived till the oxide breakdown voltage of 55 V.

Also shown in Figure 5.5 are theoretical curves obtained by assuming the complete depletion approximation for the Poly 0 surface. The value of C/C₀ was calculated according to the equation [32]:
Figure 5.5. Theoretical and experimental curves for polysilicon-to-polysilicon capacitors.
\[
\frac{C}{C_0} = \frac{1}{1 + \frac{2K_0^2 \varepsilon_0}{qN_D K_s \chi_0^2 V_G}}
\]

where

- \( \varepsilon_0 \) = permittivity of free space = 8.85 \times 10^{-14} \text{ F/cm} 
- \( K_0 \) = oxide dielectric constant = 3.75 
- \( K_s \) = silicon dielectric constant = 11.7 
- \( \chi_0 \) = oxide thickness = 850 Å 
- \( N_D \) = Poly 0 bulk concentration 
- \( q \) = electronic charge 
- \( V_G \) = applied voltage between electrodes

The following assumptions have been made, to allow for theoretical calculations to be performed:

1. Both electrodes are assumed to be single-crystalline as far as the surface and depletion regions are concerned. This is only true for small positive or negative voltages (\( \pm 10 \text{ V} \)), since for larger voltage swings, the depletion region in the Poly 0 electrode reaches the grain boundaries between the crystallites and further depletion is improbable.

2. The Poly 1 - SiO\(_2\) interface acts like a metal.

3. The Poly 0 electrode is of constant doping throughout its thickness.

4. Possible polarization effects due to phosphosilicate glass at either Si-SiO\(_2\) interface are neglected.
(5) The oxide permittivity is assumed constant.

(6) Oxide charge is neglected since after temperature and bias stress tests, negligible shift in the C-V characteristics was noted.

(7) The silicon is assumed too highly doped for inversion to take place at the fields we are considering.

In Figure 5.5, theoretical curves are drawn for different substrate doping concentrations. Also, the experimental curve is approximated by straight lines ab, bc, cd, de. It is seen that the theoretical curve for \( N_D = 3 \times 10^{18} \text{ cm}^{-3} \) and the experimental curve are in fair agreement over most of the voltage range shown. The shift in voltage, \( \Delta V = 3 \text{ V} \), is assumed to be mainly due to the net effect of the surface charge of 46.8 pC or a surface state density of \( 7.5 \times 10^{11} \text{ cm}^{-2} \). The region ab, Figure 5.5, shows that the depletion region is restricted to a finite width. At a potential of -18 V, the width of the depletion region is \( \sim 170 \text{ Å} \), assuming that the magnitude of the flatband voltage = 3 V. This restriction on the depletion width is believed to be due to the grain boundaries inside the Poly 0 electrode. The grain boundaries being regions of very high doping concentrations are assumed incapable of being depleted.

If the assumptions and theoretical calculations are correct, then a higher doping density of the Poly 0 layer is required to reduce the capacitance variation.

* At this point, the first assumption breaks down.
5.2.2 The Polysilicon-to-Silicon (Buried) Contact and Diffusion

The other structure of interest is shown in Figure 5.6. The polysilicon forms a contact to the substrate prior to the diffusion. The diode is formed by a subsequent diffusion through the polysilicon. Figure 5.7(a) shows the characteristics of one such diode of cross-sectional area $100 \times 100 \ \mu m^2$, and 1.1 $\mu m$ junction depth. The reverse breakdown voltage is about 80 V. Figure 5.7(b) shows a leakage current of less than 200 nA and a forward voltage drop of -400 mV at 1 $\mu A$. A forward current of 10 $\mu A$ requires a voltage of 500 mV. The diode has a forward dc resistance of about 250$\Omega$ at a potential of -1 V as shown in Figure 5.7(c). No contact resistance measurements between polysilicon and silicon substrate have been made. The diodes, as explained here, operate well and literature material has started to appear [10] where this kind of structure is utilized to reduce device area. LSI circuits have been fabricated, where source and drain diffusions are formed through polysilicon and where buried contacts are used instead of aluminum contacts [33], and these have been found to operate successfully.

5.3 DESIGN AND SIMULATION OF IMPROVED 4-0 SHIFT REGISTER

Figure 5.8 shows the basic layout of three cascaded capacitor pull-up inverters designed with the improved process. The input signal is applied to the gate, $G_1$, of the driver transistor of the first

* Obtained by taking the inverse of the slope at 1 V.
Figure 5.6. Polysilicon-to-polysilicon buried contact and diode formed by diffusion through polysilicon into the substrate.

inverter. The linear capacitor, $C_1$, divides the clock voltage pulse so that a high logic level appears at the drain, $D_1$, if the input gate were held at a low level, as explained in Chapter 2. This signal is passed from the drain $D_1$, via the polysilicon track to the next driver gate, $G_2$. In this manner, the signal is passed from one inverter to the next through the 'Z'-shaped polysilicon track which forms the drain contact of one inverter and the gate of the next one without any metallic contacts in between. The operation of the shift register is as explained in Chapter 2.

The inverter layout, shown in Figure 5.8, was also used to design 2-$\beta$- and 3-$\beta$ shift registers which will be described in the next Section. The photograph in Figure 5.9 shows the finished devices fabricated with the modified process of Chapter 4. Some of the tolerances
Figure 5.7. (a) Characteristics of N+ P diode obtained by diffusion of phosphorus through polysilicon into silicon.
(b) Diode leakage current.
(c) Forward dc resistance of diode.
Figure 5.8. Layout of cascaded capacitor-pull-up inverters for more optimum two-level silicon-gate process.
Figure 5.9. The photograph shows three shift registers fabricated with the modified two-level silicon-gate process for (a) 4-Φ, (b) 3-Φ, and (c) 2-Φ operation.

used in these designs are given in Table 5.2. These tolerances are larger than the state of the art in industry and have been dictated by the facilities available at the Carleton laboratories. The area of the inverters of the fabricated devices, shown in Figure 5.9, is 3 mil\(^2\) and is obtained by a centre-to-centre measurement, as shown in Figure 5.8. This area could be halved if industrial tolerances would be used, as was done in Figure 5.8.

From the design discussed above, device areas, geometries and other parameters were calculated for simulation of the expected behaviour of a 4-Φ one-bit delay. The process parameters used were the same as those used for the Nansim CCDLO process simulation program (33).
### Table 5.2. List of some minimum tolerances used in the design of one-bit delays with the modified process.

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Gate length, ( L )</td>
<td>source-to-drain separation 8 ( \mu \text{m} )</td>
</tr>
<tr>
<td>2</td>
<td>Polysilicon width</td>
<td>(a) in device well 8 ( \mu \text{m} ) (b) on field oxide 8 ( \mu \text{m} )</td>
</tr>
<tr>
<td>3</td>
<td>Polysilicon-to-polysilicon spacing</td>
<td>(a) in device well 8 ( \mu \text{m} ) (b) on field oxide 6 ( \mu \text{m} )</td>
</tr>
<tr>
<td>4</td>
<td>Polysilicon gate overlap</td>
<td>overlap over device well edge 6 ( \mu \text{m} )</td>
</tr>
<tr>
<td>5</td>
<td>Contact window area</td>
<td>(a) metal-to-polysilicon 8x8 ( \mu \text{m}^2 ) (b) polysilicon-to-silicon 8x8 ( \mu \text{m}^2 )</td>
</tr>
<tr>
<td>6</td>
<td>Metal overlap of contacts to polysilicon</td>
<td>separation between contact window edge and metal 5 ( \mu \text{m} )</td>
</tr>
<tr>
<td>7</td>
<td>*Silicon overlap of metal contact windows</td>
<td>separation of polysilicon edge and metal contact window 5 ( \mu \text{m} )</td>
</tr>
</tbody>
</table>

*Note: (5) and (7) together give the minimum size of the top electrode (Poly I) of the linear capacitor, i.e. \((18 \, \mu \text{m} \times 18 \, \mu \text{m})\).*
The clock voltages applied were the same as those used previously in the simulation of the Large-Area Device in Section 2.5, except that the applied voltage to the pull-up capacitor is now $V_+$ rather than $(V_+ - V_T)$. The model used for the inverter is the same as used in Chapter 2, altered to accommodate the new substructures. The modified model is shown in Figure 5.10. $C_L$ is the Poly 1-to-Poly 0 linear capacitance. $C_{PO}$ is the parasitic field oxide capacitance and $C_D$ is the parasitic depletion capacitance of the silicon substrate. The MOST drain and source junction, gate and peripheral capacitances are an integral part of the Nansim simulation model. The model also allows for the depletion layer capacitance below the inversion layer of the transistor when the MOST is ON. This inverter model has been cascaded four times, as was done previously in Section 2.5 to simulate a 4-$\Phi$ one-bit delay with appropriate clock voltages applied as inputs.

Computer simulation results at the output end of a one-bit delay are given in Figure 5.11(a) for 6 V and 5 V clock pulse heights. The threshold voltage is 0.5 V and no substrate bias is applied. In Figure 5.11(b), simulated results for the Small-Area Device discussed in Chapter 2 are presented here for comparison with the modified circuit. The same simulation file, Nansim CCDLO, was used for the Small-Area Device and all process parameters were recalculated to fit the new process file.

The simulation results show that the peak logic levels of the modified four-phase one-bit delay are greatly improved over those of the Small-Area Device. For 5 V clocks, the high level peak is increased from 1.64 V to 2.0 V and the low level peak is decreased from
1.5 V to 1.15 V. For the device with the modified process, the set-up time is halved, resulting in a much higher maximum frequency of operation. Higher clock voltages further improve both the high logic level peak, $V_{p0}$, and reduce the set-up time, $t_s$, of the low-level output spike, as shown in Figure 5.11(a), for 6 V clocks.

Figure 5.12 shows the simulation results for a 4-bit delay designed for the modified process with an applied substrate bias of -3 V. The effective threshold voltage is increased from 0.5 V to 1.5 V. It is important to notice that the peak zero level voltage, $V_{p0}$, is less than the threshold voltage and therefore does not restrict the frequency of operation of the device. The total set-up time is less than 10 nS.
Figure 5.11. Computer simulation results for a 4-Φ one-bit delay output with a ONE-ZERO input for (a) modified shift registers, (b) Small-Area Device (standard n-channel silicon-gate). Substrate bias voltage is zero in either case. Frequency 1 MHz; $V_T = 0.5$ V.
Figure 5.12. Simulation results for a 4-φ one-bit delay designed for the modified process with an applied substrate bias, $V_{BS} = -3 \, \text{V}$, and clock voltage, $V_0 = 10 \, \text{V}$. The equivalent threshold voltage $= 1.5 \, \text{V}$. 
An important point to notice is that when the driver MOST is ON, the value of the output capacitance $C_0$ is larger than when the MOST is OFF. This is due to the distributed capacitance beneath the MOST conducting channel. The larger value of $C_0$ helps reduce the height of $V_{p0}$ when the MOST is ON. Detailed considerations of this point are given in Appendix 1.

Computer simulation results of the modified 4-Ø one-bit delay show that the operation of this device is much better than the 4-Ø one-bit delay designed with the standard single-level silicon-gate process. Further comparisons are given in Section 5.6.

5.4 DESIGN, OPERATION AND SIMULATION RESULTS OF A 3-Ø ONE-BIT SHIFT REGISTER

In Chapter 2, it was shown that a capacitor pull-up bit delay required four cascaded inverters so that signal isolation could be achieved. This is the case for clock pulse waveforms of half duty-cycle such as in Figure 2.5. If the duty-cycle is changed so that any one clock is ON for more than half the period, $T$, then it is possible to operate a bit delay successfully with three clock pulses and three inverters per bit delay. This results in an area-reduction per bit delay, lower power dissipation and higher frequency of operation.

Figure 5.13(a) shows a circuit schematic for a three-phase capacitor pull-up one-bit delay. The associated clock voltage waveforms required are shown in Figure 5.13(b). Signal isolation is obtained because at no time are the three clocks ON at the same time. As an example, consider time slot 'A' shown in Figure 5.13(b). During this time, all inverters operating with clock $\phi_1$ are in the OFF state,
Figure 5.13. a) Circuit schematic for three-phase dynamic shift register one-bit delay.

b) Clock voltage waveforms required for operation of the circuit shown in (a).
effectively isolating all pairs of inverters operating with \( \phi_2 \) and \( \phi_3 \) clocks and allowing those inverters operating with the \( \phi_3 \) clock to develop the relevant logic state. The signal progresses through the shift register in the same manner as discussed in Chapter 2 for the 4-Ø shift register. However, in three-phase operation, the logic level is maintained for a longer time, i.e. \( 2/3 \ T \) and not \( 1/2 \ T \), as in the 4-Ø bit delay, where \( T \) is the clock pulse period. Another main difference is that after one-bit delay \( V_{\text{out}} \) is the negative of \( V_{\text{in}} \) or if the input signal was a high logic level, the output signal after a bit delay is a low logic level.

Computer-simulated output results for a 3-Ø one-bit delay are shown in Figure 5.14 for 5 V and 6 V clocks and a ONE-ZERO input. The same circuit model as in Figure 5.10 is used and the element values are the same as for the 4-Ø modified shift register. The simulation file, Nansim CCDLO, was used. The clock pulse waveforms are included in the Figure for ease of explanation. Time slots \( t_1, t_2, \ldots, t_6 \) represent the times during which changes are occurring in the output signal levels.

During time slot \( t_1 \), the high logic level is formed, the inverse of the ZERO input word delayed by one-bit. It is noted that the peak value \( V_{p1} \) is 2.1 V and 2.4 V for 5V and 6 V clocks respectively. These values are higher than for the 4-Ø device, Figure 5.11(a), because the initial drain potential is less negative for 3-Ø operation than for 4-Ø operation. This is explained later. The voltage feed-through effects due to the \( \phi_2 \) clock going OFF are seen in time slots.
Figure 5.14. Computer simulated results for a 3-Φ one-bit delay output with a ONE-ZERO input word. Substrate bias, $V_{BS}=0$; Frequency=1 MHz; $V_c=0.5$ V. The top three traces represent the $\phi_1$, $\phi_2$ and $\phi_3$ overlapping clocks.
and \( t_5 \). During the fall time of the \( \phi_3 \) clock, the clock \( \phi_2 \) is rising and develops either a logic ONE (time slot, \( t_3 \)) or a logic ZERO (time slot, \( t_6 \)). During \( t_3 \), the logic ONE that appears on the gate of the output MOST limits the excursion of the drain potential beyond ground to a very small value. After a few nanoseconds, the drain is grounded. During time slot \( t_6 \), the logic ZERO appearing on the gate turns on the output MOST for a short while. At this time, the potential of the drain is at its largest negative value. Charge from the drain diffusion flows to the grounded source as explained in Chapter 2. However, because the gate is ON, more charge flows to ground than is the case with the 4-\( \phi \) shift register. The negative potential of the drain is therefore reduced to a smaller value in a shorter time interval, as is evident by comparing time slots \( t_6 \) of Figures 5.11(a) and 5.14.

The operation of the 3-\( \phi \) bit delay is thus basically similar to the operation of a 4-\( \phi \) bit delay, but the resulting signal levels are better.

5.5 DESIGN, OPERATION, SIMULATION AND EXPERIMENTAL RESULTS OF 2-\( \phi \) OPERATION

With the capacitor as the pull-up element, the input level must be held stable during the set-up time, \( t_s \) (Figure 2.2) of Chapter 2. As soon as the data has been passed along to the following stage, the input data can change even though the clock is still at its high level because the output can only respond to a low to high transition at the input by discharging the high level output to a low level through the driver MOST. When the input changes from high to low, however, the
output remains at low since no current is available to charge up the output capacitor \( C_0 \). Therefore, it is possible to drive two cascaded inverters by one clock provided that the peak voltage of the low level output \( V_{p0} \), Figure 2.2) of the first inverter is less than the threshold voltage of the driver MOST.

In Figure 5.15, the two stages are driven by \( \phi \), the clock. \( \bar{Q} \) is the inverted output of DATA IN and \( \bar{Q} \) is the complement of \( Q \) and has the same logic state of DATA IN delayed by the set-up time, \( t_{s2} \), of the second stage. Notice that the DATA IN can change as soon as the data is valid at the \( \bar{Q} \) output.

Figure 5.16 shows a circuit schematic of a one-bit two-phase dynamic shift register using overlapping clock pulses and the associated clock voltage waveforms required to operate it. The one-bit delay consists of two double-stage gates cascaded in the manner shown in Figure 5.16(a). The clock waveforms must be similar to those shown in Figure 5.16(b). To show the differences in operating this shift register from the previous ones described, computer simulation results on a one-bit delay are obtained by using the inverter model shown in Figure 5.10. All parameters of the inverters are the same as used in the simulations of the modified 4-\( \phi \) and 3-\( \phi \) one-bit delays. The simulation results for nodes 5, 6, 7, 8 (Figure 5.16(a)) showing the progression of a ONE-ZERO input through the one-bit delay as well as the clock waveforms and the input voltage are shown in Figure 5.17. The threshold voltage, \( V_T \), is 0.5 \( V \) and the clock pulse heights are 5 \( V \) each. No substrate bias is used.
Figure 5.15. Schematic of a double-stage single clock logic gate and the various nodal waveforms.
Figure 5.16. (a) Circuit schematic of a one-bit two-phase dynamic shift register using overlapping clock pulses.

(b) Clock voltage waveforms required for the circuit shown in (a).
Figure 5.17. Simulation results showing the progression of a ONE-ZERO input through a 2-ϕ one-bit delay. Also shown (top three traces) are the clock waveforms, $\phi_A$ and $\phi_B$, and input voltage, $V_{in}$. 
In unison with the rise time of $\phi_1$, both the potentials of node 5 and node 6 rise to develop a logic ZERO and a logic ONE, respectively. The ZERO-level spike, of height $V_{p0}$, on node 5 causes a slight discharge of the high level, $V_{p1}$, on node 6, seen in time slot $t_0$. This is because the voltage spike is above $V_T$ for a very short time.

If the value of $V_{p0}$ is much higher than the threshold voltage, $V_T$, and the set-up time, $t_s$, is too long, then the discharge of the high voltage level, $V_{p1}$, will be seriously degraded and the device will require higher clock voltages to operate successfully. It should be noted that the high level on node 6 is maintained till the fall time of $\phi_A$, time slot $t_1$, i.e. for a time equal to the ON-time of the $\phi_A$ clock.

During time slot $t_2$, in unison with the rise time of $\phi_A$, a high level is developed on node 5 and a low level on node 6. There is no discharge of the high logic level on node 5 because the ZERO level on the previous node is formed one-half period earlier. The corresponding low level spike formed on node 6 has a larger set-up time, $t_s$, because the driver MOSFET comes ON during the clock rise time and therefore discharge to ground starts later than for the case of the 3-0 and the 4-0 devices. Also, because $V_{in}$ comes ON during time slot $t_3$, node 5 is discharged to ground at this time and not during the fall time of $\phi_A$. Hence, if the input is high, a logic level representing a logic ONE is only ON for half the clock period on the output drain of the first gate of a double-stage single-clock gate. This is seen to be the case in nodes 5 and 7. During time slot $t_3$, the fall time of the high level on node 5 coincides with the rise time of the high level.
on node 7. Each high level is equal to half the clock period and the high levels on node 5 and node 7 no longer overlap each other. Hence, it is impossible to use single inverter stages for 2-Ø operation. The use of double-stages allows the high logic levels to regain an ON-time equivalent to the ON-time of the clocks, and since these are overlapping, signal progression through a shift register is possible.

The experimental 4-Ø shift registers described in Section 2.4 of Chapter 2 can be used to achieve the two-phase operation described here by using two-phase overlapping clocks with one clock, \( \phi_A \), connected to the \( \phi_1 \) and \( \phi_2 \) lines and the other, \( \phi_B \), connected to the \( \phi_3 \) and \( \phi_4 \) lines. The overlap time is required to be not less than the longest set-up time of the four stages. The standard single-level silicon-gate MOS Large-Area Device of Chapter 2, with 0.36 V threshold voltage, is shown operating with two-phase overlapping clocks at 1 MHz in Figure 5.18. With a typical set-up time of 20 nS, high frequency operation up to 16 MHz was experimentally observed. Operating at higher frequencies is also possible, but was limited by the clock drivers. The high frequency limit for two-phase operation is expected to be comparable to that of the four-phase operation.

5.6 COMPARISON BETWEEN 2-Ø, 3-Ø AND 4-Ø SHIFT REGISTERS

The simulation results presented in the previous Sections of this Chapter are now compared to each other. Comparisons of these shift registers to the Small-Area Device described in Chapter 2 are made. Some improvements that are possible with tolerances comparable to those used in industry are pointed out.
In Table 5.3 are given relevant areas pertaining to the Small-Area Device and the 2-Ø, 3-Ø and 4-Ø versions of this device designed with the modified process. Also given are possible improved values of these areas. These improvements are achieved by using the following tolerances instead of 3b, 5a and 7 given in Table 5.2:

Polysilicon-to-polysilicon spacing on field oxide = 4 μm

Metal-to-polysilicon contact window area = 6 x 6 μm²

Silicon overlap of metal contact windows = 4 μm

It should be noted that the area of the modified shift registers shown in Table 5.3 cannot be compared directly to those of the Small-Area
Table 5.3. Relevant information about the geometries of capacitor pull-up shift registers.

<table>
<thead>
<tr>
<th>UNIT</th>
<th>SMALL AREA DEVICE</th>
<th>MODIFIED SHIFT REGISTERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area of load capacitor, $C_L$</td>
<td>$\mu m^2$</td>
<td>816 324 324 324 196</td>
</tr>
<tr>
<td>Area of drain diffusion</td>
<td>$\mu m^2$</td>
<td>224 108 108 108 -</td>
</tr>
<tr>
<td>Periphery of drain junction</td>
<td>$\mu m$</td>
<td>60 52 52 52 -</td>
</tr>
<tr>
<td>MOST aspect ratio, W/L</td>
<td>-</td>
<td>1.75 1.5 1.5 1.5 1</td>
</tr>
<tr>
<td>Gate length, L</td>
<td>$\mu m$</td>
<td>8 8 8 8 -</td>
</tr>
<tr>
<td>Area per inverter</td>
<td>mil$^2$</td>
<td>3.87 3 3 3 1.9</td>
</tr>
<tr>
<td>Area per bit delay</td>
<td>mil$^2$</td>
<td>15.50 12 9 12 7.6**</td>
</tr>
</tbody>
</table>

*Expected values with standard tolerances.
**This area is for a 4-Ø shift register one-bit delay. For a 3-Ø one-bit delay, the area is 5.7 mil$^2$. 
Device since the latter was designed for an industrial process. The figures shown in the last column are more representative of an industrial process. A further significant area improvement can be achieved in the 2-Φ version because for the double-stage gate discussed previously, the top electrode of each load capacitor may be implemented by a single electrode as shown in Figure 5.19. This requires much less area to implement. With a suitable design layout, a large number of metal-to-polysilicon contacts can be eliminated.

Values of capacitive elements of the inverters are given in Table 5.4. It is seen that in the modified version of the shift registers, the total capacitance (C_L + C_o) is less than one-half that of the Small-Area Device. This results in lower power dissipation and increased frequency of operation as is shown in Table 5.5. The first four rows are simulation values while the last two rows are calculated.
Table 5.4. Values of capacitances for the inverter geometries given in Table 5.3. All units are in pF.

<table>
<thead>
<tr>
<th></th>
<th>SMALL AREA DEVICE</th>
<th>MODIFIED S/R ONE-BIT DELAY</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2-Ø</td>
<td>3-Ø</td>
</tr>
<tr>
<td>Value of load capacitor, ( C_L )</td>
<td>0.2448</td>
<td>0.0972</td>
</tr>
<tr>
<td>Drain junction area capacitance, ( C_{ja} )</td>
<td>0.0246</td>
<td>0.0205</td>
</tr>
<tr>
<td>Drain junction peripheral capacitance, ( C_{jp} )</td>
<td>0.036</td>
<td>0.0312</td>
</tr>
<tr>
<td>MOST gate capacitance, ( C_g )</td>
<td>0.0336</td>
<td>0.0288</td>
</tr>
<tr>
<td>Parasitic capacitance in series with ( C_L ) and below it</td>
<td>-</td>
<td>0.063</td>
</tr>
<tr>
<td>Depletion capacitance below gate of conducting MOST</td>
<td>0.155</td>
<td>0.2</td>
</tr>
<tr>
<td>Depletion capacitance below gate of conducting MOST</td>
<td>0.061</td>
<td>0.0523</td>
</tr>
<tr>
<td>Total output capacitance, ( C_0 )</td>
<td>0.328</td>
<td>0.18</td>
</tr>
<tr>
<td>Capacitive divider ratio, ( \frac{C_L}{C_L+C_0} )</td>
<td>0.427</td>
<td>0.351</td>
</tr>
<tr>
<td></td>
<td>0.478</td>
<td>0.432</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.418</td>
</tr>
</tbody>
</table>

* Expected values with standard tolerances.
Table 5.5. Comparative operational characteristics of modified 2-∅, 3-∅ and 4-∅ shift registers and Small-Area Device.

<table>
<thead>
<tr>
<th>UNIT</th>
<th>SMALL AREA DEVICE</th>
<th>MODIFIED S/REGISTERS</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>2-∅**</td>
<td>3-∅</td>
</tr>
<tr>
<td>Peak value of high logic level, $V_p$</td>
<td>V</td>
<td>1.6</td>
<td>2</td>
</tr>
<tr>
<td>Peak value of low logic level, $V_{p0}$</td>
<td>V</td>
<td>1.5</td>
<td>1.15</td>
</tr>
<tr>
<td>Set-up time, $t_s$</td>
<td>nS</td>
<td>28</td>
<td>16</td>
</tr>
<tr>
<td>Propagation delay. Time for low logic level to discharge below $V_T$</td>
<td>nS</td>
<td>13</td>
<td>4</td>
</tr>
</tbody>
</table>
| Minimum clock voltage required to operate devices. | V       | 2.05     | 1.65   | 1.65    | 1.65 | 1.7  | - | $V_{min}$
| $CV_f^2$ power consumed per inverter at 1 MHz | μW      | 12.8     | 5.6    | 5.6     | 5.6  | 3.5  | $V_{min}$=5\,V |
| | μW      | 2.2      | 0.6    | 0.6     | 0.6  | 0.4  | $V_{min}$=5\,V |

* Expected values with standard tolerances.
** The first value refers to the first inverter of the double-stage gate while the second value refers to the second inverter.
*** $V_{min} = V_T\left(\frac{C_L+C_O}{C_L}\right) + 0.5 + V_T$; for Small-Area Device

$V_{min} = V_T\left(\frac{C_L+C_O}{C_L}\right) + 0.5$; for modified shift registers.
Using the time required for the low logic level to discharge to a value below the threshold voltage, $V_t$, as a basis for calculating the maximum frequency of operation, then the maximum delay in a 4-$\Phi$ one-bit delay is $(4 \times 4 \text{ nS}) = 16 \text{ nS}$. Then, the theoretical maximum frequency of operation for the modified shift registers is about 60 MHz. This calculation is only theoretical and ignores the effect of the clock rise and fall times on the frequency.

5.7 CONCLUSIONS

The theoretical and experimental results of the polysilicon-to-polysilicon capacitor and the polysilicon-to-silicon contact have been presented. A mask design was carried out to obtain the relevant areas and geometries of elements and structures so that one-bit delays could be simulated. Fabrication test runs were performed and the processing procedure was found to be feasible. A modern computer simulation program, Nansim CCDLO, developed by Bell-Northern Research [5], was used for the simulation of 2-$\Phi$, 3-$\Phi$, and 4-$\Phi$ one-bit delays. Simulation results of the Small-Area Device discussed in previous Chapters were also presented. These results show that the shift registers design with the modified process are smaller in area, dissipate less power and are capable of operating at higher frequencies.
CHAPTER 6
CAPACITOR PULL-UP CIRCUIT APPLICATIONS AND COMPARISON TO OTHER CIRCUITS

6.1 INTRODUCTION

The theory and analysis of capacitor pull-up circuits has been investigated in terms of the basic capacitor pull-up inverter and in terms of shift register one-bit delays which are obtained by directly cascading four (or three) such inverters. Designs of shift registers have been discussed and experimental and computer simulation results have been presented. The development of a process for improved devices has been considered and computer simulation results of the modified devices have shown an improvement in the overall circuit performance.

The results that have been presented, and the discussion following, show that, while capacitor pull-up circuitry might not be indicated for general purpose design of random logic circuits, it is nevertheless an important tool to consider in specific contexts. The fact that capacitor pull-up circuitry is realizable with standard MOS processes allows it to be implemented along with other circuitry with no additional processing steps. Hence, possible applications of capacitor pull-up circuits are discussed in Section 6.2. Applications for shift-registers, general logic and peripheral support circuitry for larger circuits are presented. In Section 6.3, an attempt is made to place capacitor pull-up circuits in context with another technology, viz. I^2L. Section 6.4 concludes the Chapter.
6.2 POSSIBLE APPLICATIONS OF CAPACITOR PULL-UP CIRCUITRY

6.2.1 Shift Register Applications

Shift registers seem to be the most obvious application of capacitor pull-up circuitry. It has been demonstrated that two-phase, three-phase and four-phase shift registers operating at higher than conventional speeds are easily realizable with a standard single-level n-channel silicon-gate process. A double-level polysilicon-gate process provides further improved performance, especially if modified to include the polysilicon-to-polysilicon capacitor and buried contacts. Important advantages, besides the high frequency of operation, are the simplicity of structure and the low power dissipation. Table 6.1 shows the performance data of commercially available shift registers*. The shift registers that had the highest frequency of operation for the particular technology were chosen for comparison. All the shift registers are 1024 bits long, serial-input serial-output, and all are fabricated using MOS silicon-gate processes. The last three shift registers shown are capacitor pull-up shift registers, including the standard silicon-gate n-channel Small-Area Device, discussed in Chapter 2, and the modified 4-∅ and 3-∅ shift registers, as designed for the improved process. The threshold voltage for the capacitor pull-up

* This information is taken from "MSI-LSI Memory DATA Book", by D.A.T.A. Inc., Autumn 1975.
Table 6.1. Shift register performance data comparison for 1024-bit shift registers.

<table>
<thead>
<tr>
<th>TYPE NUMBER</th>
<th>NUMBER OF REGISTERS</th>
<th>TECHNOLOGY</th>
<th>MAX. FREQ. OF OPERATION (MHz)</th>
<th>MAXIMUM POWER DISSIPATION (mW)</th>
<th>RATED POWER SUPPLIES -ve +ve</th>
<th>INPUT LOGIC LEVELS MAX. ZERO MIN. ONE</th>
<th>MAXIMUM PROPAGATION DELAY (nS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCD450ADC</td>
<td>9</td>
<td>CCD(N)</td>
<td>2</td>
<td>250</td>
<td>2.5V 12V</td>
<td>.8V 2.2V</td>
<td>140</td>
</tr>
<tr>
<td>AM2533DC</td>
<td>1</td>
<td>STATIC(P)</td>
<td>1.5</td>
<td>150</td>
<td>12V 5V</td>
<td>.8V 2V</td>
<td>300</td>
</tr>
<tr>
<td>M43404</td>
<td>1</td>
<td>DYNAMIC(P)</td>
<td>10</td>
<td>500</td>
<td>5V 5V</td>
<td>.8V 3V</td>
<td>90</td>
</tr>
<tr>
<td>M45026D</td>
<td>2</td>
<td>DYNAMIC(P)</td>
<td>3</td>
<td>409</td>
<td>12V 5V</td>
<td>.8V 3.3V</td>
<td>90</td>
</tr>
<tr>
<td>SMALL-AREA DEVICE 4-Ø</td>
<td>1</td>
<td>DYNAMIC(N)</td>
<td>20</td>
<td>52*</td>
<td>2V -</td>
<td>.7V 2.4V</td>
<td>13</td>
</tr>
<tr>
<td>MODIFIED 4-Ø</td>
<td>1</td>
<td>DYNAMIC(N)</td>
<td>60</td>
<td>23*</td>
<td>- -</td>
<td>.25V 1V</td>
<td>4</td>
</tr>
<tr>
<td>MODIFIED 3-Ø</td>
<td>1</td>
<td>DYNAMIC(N)</td>
<td>80</td>
<td>17*</td>
<td>- -</td>
<td>.25V 1V</td>
<td>3.5</td>
</tr>
</tbody>
</table>

* Excludes power required for development of clocks on chip and output circuitry. These values are calculated according to $CV^2f$ at 1 MHz required from all clocks together required to drive 1024 bits. The comparison with the commercial devices is not straightforward because the specifications of the commercial devices include allowances for manufacturing tolerances. The power dissipation of the commercial devices includes power for peripheral circuitry.

** To compensate for the allowance of manufacturing tolerances of commercial devices, the calculated operating frequencies for the capacitor pull-up devices have been specified conservatively, e.g., the Small-Area Device has been operated at 34.5 MHz.
shift registers is assumed to be 0.5 V and the height of the required clock pulses are 5 V. For the other cases shown in Table 5.1, the clocks are incorporated on the chip itself and only d.c. supplies are required externally. The values of maximum power dissipation shown for the capacitor pull-up registers are calculated as follows:

\[
[(\text{Total # of inverters}) \times (CV^2f \text{ power per inverter})]
\]

The power required by the support circuitry to develop these clocks as well as the power dissipated by the output devices are not included in the figures shown.

The Small-Area Device was operated at 20 MHz with 5 V clocks and -2 V substrate bias. The experimentally measured values for the maximum ZERO logic level and the minimum ONE level were 1.2 V and 1.7 V respectively. The values shown in Table 6.1 are more conservative. The maximum propagation delay is obtained from computer simulation results performed and does not include the clock rise time or fall time. It is understood that for the higher frequencies shown the pulse rise times and fall times must be less than 5 nS.

All the data shown for the modified four-phase and the modified three-phase capacitor pull-up shift registers are obtained from computer simulation results of one-bit delays designed for the improved capacitor pull-up process, as explained in Chapter 5. Further improvements are possible if industrial tolerances are used. The clock voltage heights are 5 V and no substrate bias is applied.

One major improvement of using the improved capacitor pull-up process instead of the standard single-level silicon-gate process
is the reduction in capacitance that each clock is required to drive. This is important in the sense that clock drivers are limited at high frequencies by the capacitance they are required to drive. Using the capacitance values given in Table 5.4 of Chapter 5, it is seen that for a 1024-bit standard silicon-gate NMOS capacitor pull-up shift register, an extension of the Small-Area Device, each of the clocks is required to drive a maximum of 600 pF. For the case of the shift registers designed with the new improved process, the clocks are required to drive a maximum of 300 pF. If industrial tolerances were used, this input capacitance would be less than 200 pF.

From the data shown in Table 6.1, it is seen that the maximum frequency of operation is much higher than that of any commercially available shift register of the same length, while the propagation delay is very small indeed. These two characteristics can be applied to advantage in particular circumstances, as will now be discussed.

6.2.2 Timing and Demultiplexing Applications

In Chapter 2, it was stated that the original motivation for this work was to find a digital logic circuit which operates on the same clocks and the same process parameters as CCDs, to be used for peripheral logic on a CCD chip, saving the necessity for a separate set-up for clocks.

A double poly-Si process developed in Bell-Northern Research [9] can be used to fabricate charge-coupled devices [34] in addition to conventional Si-gate MOS circuits. Since the capacitor pull-up circuit can be operated by using the same drive requirements as the charge-
coupled devices, namely, overlapping multi-phase clocks and a substrate bias [35,36], it is possible to design the capacitor pull-up circuit on the CCD chip to provide peripheral logic such as multiplexing, decoding and timing. On the CCD chip, the capacitor pull-up circuit has the advantages of high speed and simple drive requirements. More conventional dynamic MOS logic circuits fabricated on the same chip as CCD's usually require different drive waveforms than those used by the CCDs.

Consider the schematic diagram of Figure 6.1, where a capacitor pull-up shift register is used as a timing circuit to demultiplex an input analog signal into, for example, CCD shift registers. The necessity to demultiplex may be due to a variety of reasons such as the lower frequency of operation of CCD shift registers, or because the driving circuitry is not capable of driving the heavy output capacitive loading due to CCDs. On the other hand, one would still want to use CCDs because of their high circuit density. Demultiplexing would then allow the input analog signal to be sampled at a very high frequency, while each sample is shifted through the shift registers at a much lower frequency. For a logical ONE shifting through the capacitor pull-up shift register, each of the MOST gates shown is sampled consecutively, and the input signal is thus effectively demultiplexed at high speed.

In some cases, the total area of the circuit is strongly dependent on the shift register pitch*, which for the case shown in Figure 6.1

* Private communication with Marvin White.
is the separation between any two $1/2$ bit delays of the capacitor pull-up shift register. For the modified shift registers, pitches of the order of $22 \, \mu m$ may be achieved. This application is ideal for capacitor pull-up circuitry because of the small loading required at every output. Under such conditions, the shift register will be able to maintain its high frequency of operation and low power dissipation. A very important point to note here is that the high outputs of the shift registers representing a logic ONE are obtained as fast as the clock rise time, since the output levels rise in unison with the clocks (Chapter 2). Hence, for a particular frequency and clock pulse rise
time, the MOST gates—shown in Figure 6.1—are turned ON after a minimum delay which is less than the clock rise time. This is a desirable mode of operation.

6.2.3 Decoding Applications

In Chapter 5, the theory of two-phase operation was discussed and computer simulation and experimental results were presented. This mode of operation was possible because two cascaded inverters can run off the same clock allowing both the Q and \( \overline{Q} \) outputs to be present simultaneously, Figure 5.15, Chapter 5. As a result, an extremely fast decode circuit is possible (Figure 6.2). Shown symbolically is a 3-input NAND gate, an inverter and three signal lines. The \( \overline{A}, \overline{B} \) and \( \overline{C} \) lines are assumed removed, at an area saving, and the inversion required are developed at the point in the circuit where necessary. Here the decoder is developing \( \overline{ABC} \). The inversion is developed by the same clock which powers the NAND gate. The NAND gate is shown using the capacitor pull-up inverter as the basis of the NAND function. If the output spike of the NAND gate for a low level output is held below threshold, the result of the decoder is valid almost as fast as the clock can rise.

6.2.4 Random Logic Applications

Since general logic is performed by inverter gates together with series/parallel input gates, therefore the capacitor pull-up technique can also be extended for general logic. An example of this is the modulo-8 counter shown in Figure 6.3 and the capacitor pull-up version of the counter shown in Figure 6.4. This circuit was breadboarded and
operated with two-phase, three-phase and four-phase overlapping clocks at frequencies up to 8 MHz.

In a random logic application, the output load capacitance tends to vary from one gate to another, that is, the output capacitance of a three-input NAND gate is much higher than that of a single inverter stage. This higher capacitance increases the set-up time and reduces the frequency of operation of the device, making random logic less attractive for capacitor pull-up. Moreover, nowadays, there is a strong tendency to exchange random logic arrays with Programmable Logic Arrays (PLAS) and Read Only Memories (ROMS) because of the high
Figure 6.3. Block diagram of modulo-8 counter using D-type flip-flops.
(After Booth, Ref. 37, p. 213)
Figure 6.4. Realization of the modulo-8 counter of Figure 6.3, using capacitor pull-up logic.
design cost of random logic. In some cases, hardware is also being traded for software as in microprocessors. Hence, random logic is of decreased general interest. However, in the context of a general logic application, capacitor pull-up logic might be useful for a local high frequency logic circuit, for example, for a counter developing high frequency timing pulses for slower logic elsewhere in the chip.

In general, capacitor pull-up logic has possible applications as high speed shift registers and as peripheral support circuitry for LSI's, wherever it is required to drive small capacitive loads. In these cases, capacitor pull-up circuits provide high-speed operation, fast-access times, low power dissipation and small propagation delays.

6.3 COMPARISON TO $I^2$L TECHNOLOGY

When logic technologies are compared to each other, it is customary to look at the propagation delay and power dissipation per gate. This comparison is not necessarily meaningful for all technologies since static power, dynamic power, power dissipation due to leakage or a mixture of these are not easily related. Hence, before comparing values of the power dissipation and propagation delay, these values shall be explained in the light of capacitor pull-up logic.

In Figure 6.5 are shown the possible outputs of a capacitor pull-up inverter for an applied clock pulse of height $V_\phi$. The clock rise time, $t_r$, shown is typically 5 nS or less and the impedance of the MOS capacitor dielectric is assumed to be greater than $10^{-14}$ Ω. The high output logic ONE is assumed valid as soon as the output voltage $V_{out} > V_T$, and hence the associated propagation delay, $t_{pd}$, is less than
Figure 6.5. The propagation delay time, \( t_{pd} \), the inverter set-up time, \( t_s \), and the clock pulse rise time, \( t_r \), are shown for a capacitor pull-up inverter.

(a) a high logic level output with \( V_{p1} > V_T \). Here, \( t_s = t_r \).
(b) a low logic level output with \( V_{p0} < V_T \).
(c) a low logic level output with \( V_{p0} < V_T \) where \( V_T \) is the device threshold voltage and \( V_\phi \) is the clock pulse height.
the rise time, \( t_r \), Figure 6.5(a). The set-up time, \( t_s = t_r \), and both \( t_s \) and \( t_{pd} \) are dependent on the clock rise time. In Figures 6.5(b) and (c) are shown the inverter low level outputs representing a logic ZERO. In the former, the peak output voltage \( V_{p0} > V_T \), and hence the output is valid at \( t_{pd} > t_r \), i.e. when the output capacitance has discharged to a voltage equal to the threshold \( V_T \). In Figure 6.5(c), the peak output ZERO level, \( V_{p0} \), never reaches the threshold voltage and the output voltage is consequently valid instantaneously, i.e. \( t_{pd} = 0 \). Note that the transient spike shown in (b) and (c) does not affect signal propagation in any way.

For comparison to another logic technology, the worst case values of \( t_{pd} \), as per Figure 6.5, will be used assuming the clock rise time is 5 ns. The output voltage values are obtained from computer simulation results obtained in the manner discussed in Chapter 5 for the modified shift registers designed for the more optimum process and for the standard silicon-gate n-channel Small-Area Device.

The power dissipation per gate is calculated for the capacitor pull-up devices according to the equation \( CV^2f \), where \( C \) is the maximum total inverter capacitance loading the clock, i.e. \( C = (C_L + C_O) \) at 0 V, \( V \) is the clock pulse height, \( V_f \), and \( f \) is the frequency of operation.

Figure 6.6 gives a comparison between an \( I^2L \) inverter and various capacitor pull-up inverters. It shows the delay per inverter gate plotted against the power dissipation per inverter. The data shown for the \( I^2L \) inverter, curve 1, is provided by Berger and Wiedman [38]. This data was experimentally obtained from a 7-stage recirculating inverter chain. Experimental observations were averaged to give
Figure 6.6. Average delay versus power dissipation for single inverter stages for (1) $I^2L$ inverter; (2) standard n-channel silicon-gate inverter with $V_T=0.1 \, \text{V}, \, V_{BS}=0 \, \text{V}$; (3) standard n-channel silicon-gate inverter with $V_T=0.1 \, \text{V}, \, V_{BS}=-1.0 \, \text{V}$; (4) inverter designed with the new improved double polysilicon-gate process, $V_T=0.5 \, \text{V}$. The reason for the above choice of $I^2L$ values is given in the footnote on p. 117.
the power dissipation and propagation delay per inverter. Curve 2 represents the experimentally measured data for the standard Small-Area Device with a threshold voltage of 0.1 V and no substrate bias. The shift register consists of a chain of 64 inverters and the experimental values shown are average values for a single inverter stage. The experimental results shown in Curve 3 are for the same Small-Area Device with a substrate bias of -1 V. This raises the effective threshold voltage to about 0.6 V. Curve 4 shows computer simulation results for a single inverter of a modified 4-Ø, one-bit delay using the more optimum process described in Chapter 4, with a threshold voltage of 0.5 V and no substrate bias. The differences seen in Curves 2 and 3 for the Small-Area Device would be reflected with the use of a substrate bias, in Curve 4 also.

The capacitor pull-up curves are compared to the power delay curve given by Berger and Wiedmann, because these $I^2L$ inverter power-delay values were averaged from experimental results obtained over a seven-inverter chain. This method is therefore similar to the way the power-delay values for a capacitor pull-up inverter were obtained, since these also were averaged over a cascaded-inverter chain.

* Since the publication of Reference 38 by Berger and Wiedmann, in 1972, various other papers [39-42] have been published about $I^2L$. It is shown in the more recent literature that $I^2L$ has power-delay values that are about an order of magnitude better than the values shown in Figure 6.6. However, the curve shown (curve 1) was chosen here because the comparison is being made with equivalent processing tolerances. If tighter industrial tolerances were used for the modified shift registers (curve 4), the power-delay values would be further improved. In a recent paper by Altman (8), April 1976, the $I^2L$ technology is compared to the double-level polysilicon-gate n-channel process, as well as to other MOS processes.
The curves in Figure 6.6 show that the Standard silicon-gate n-channel Small-Area Device with a small substrate bias has power-delay curves that are comparable to the \( I^2L \) values shown. A big improvement is shown for the capacitor pull-up inverter implemented by the two-level polysilicon process modified to include the substructures described in Chapter 4. It should be noted that, for the latter inverter, increasing the clock voltage height beyond that required to make \( V_{d0} < V_T \) does not alter the inverter propagation delay significantly, as seen from Figures 6.5(a) and (c), and hence Curve 4 shown in Figure 6.6 tends to flatten out at higher power levels. It should also be noted that all capacitor pull-up values shown in Figure 6.6 assume clock pulse rise times of 5 ns. Faster clock rise times reduce the delay per gate. For inverter designs with smaller tolerances as are used in industry, it is expected that the power dissipation values required for successful operation would be greatly improved over the values shown in Figure 6.6.

The area required for implementation of one-bit delay of the standard silicon-gate Small-Area Device is 15 mil\(^2\) (Table 5.3). If two inverters per bit delay are assumed for the \( I^2L \) technology, then the area required per bit delay with the \( I^2L \) process is about 8 mil\(^2\), as reported by Hart and Slob and others [38-42]. For the capacitor

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* Reference is made to Table 5.5 of Chapter 5 where, for minimum clock voltage operation at 1 MHz, the \( CV^2f \) power dissipation per inverter is estimated to be 0.4 \( \mu \)W per inverter or an energy dissipation of 0.4 pJ.
pull-up bit delays designed with the double-level n-channel silicon-gate process of Chapter 4, the area-per bit delay is \(9 \text{ mil}^2\), for 3-\(\phi\) operation, and 12 \text{ mil}^2 for 2-\(\phi\) and 4-\(\phi\) operation (Table 5.3), which compares favourably with the values given for \(I^2L\). The tolerances used for these \(I^2L\) geometries are as follows:

- 0.3 mil, metal line width;
- 0.15 mil, spacing and
- 0.2x0.2 mil\(^2\)

contact holes [38-40]. These tolerances are smaller than the ones used for the design of the capacitor pull-up bit delays. It should be noted that for the inverter designed with standard industrial tolerances and a double-polysilicon process, the area was estimated to be 1.9 mil\(^2\) (Table 5.3), i.e. 5.7 mil\(^2\) and 7.6 mil\(^2\) for a 3-\(\phi\) and 4-\(\phi\) bit delay, respectively. The capacitor pull-up one-bit delay would therefore seem to be smaller than the one-bit delay achievable with the \(I^2L\) process, as described in the references given above. Improved \(I^2L\) processing, for example using LOMOS processes [41], have resulted in slightly denser circuits than have been reported here. A comparison between MOS and \(I^2L\) processing and resulting circuitry has been given by Altman [8], and here the standard n-channel double-polysilicon gate process was compared directly to the double-level \(I^2L\) process. The double-polysilicon process is shown to be slightly denser than the \(I^2L\) process in this paper, while \(I^2L\) was reported to have better power-delay characteristics.

* These comparisons were made for standard logic techniques and not capacitor pull-up logic.
In proposing new circuit and processing techniques, such as capacitor pull-up logic designed with the modified two-level polysilicon process, it is necessary to compare the novel circuits and processes to established ones. In doing so, one often uses the propagation-delay, the power-delay product, the density and the chip size as criteria for comparison. When comparing the density of gates achievable with a process A, to the density of gates achievable with another process B, it is often found that one particular circuit might be more readily implemented with process A than with process B. On the other hand, another circuit might produce a higher density of gates per unit area when designed with process B than with process A. Hence, a comparison of gate densities for different processes can only be made for one particular circuit. In the comparison given above, the dynamic capacitor pull-up inverter was compared to the static \( I^2L \) inverter, without considering the need of providing clocks for running the capacitor pull-up logic. This will be discussed in Chapter 7.

6.4 **CONCLUSIONS**

Possible applications of capacitor pull-up circuits have been discussed. It was demonstrated that shift registers built using this technique are capable of being operated at frequencies which are much higher than is available with other MOS technologies. The overall improvement in performance of capacitor pull-up logic designed with a modified two-level polysilicon-gate process rather than with a single-level silicon-gate n-channel process has been explored. It has been shown that this logic circuitry can be used for peripheral support
circuitry on larger chips for decoding, timing and demultiplexing. In this context, the capacitor pull-up technique has the advantage of very fast access times and short propagation delays, besides low power dissipation. The propagation delay and power dissipation of the capacitor pull-up inverter are comparable to those for the I^2L inverter, when the standard silicon-gate n-channel process is used. For the modified double-level polysilicon process, the capacitor pull-up inverter has a better power-delay product than the inverter designed with the standard silicon-gate process.
CHAPTER 7

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

The use of an MOS capacitor as an integrated logic load element for dynamic MOS LSI circuits instead of the more common MOS load transistor has been investigated and reported in this thesis.

The standard silicon-gate n-channel process was used originally to fabricate two shift registers incorporating a particular approach for the capacitor pull-up element, which was implemented as a varactor. The two shift registers were extensively tested for high frequency and minimum clock voltage operation for a wide range of threshold voltage. The theory of operation of capacitor pull-up one-bit delays employing overlapping clock pulses was hence established, and the effect of substrate bias on device behaviour was investigated and reported. Computer simulation results were found to be in agreement with the experimental results obtained. At this stage, the results available were published in an IEEE Electron Device Conference Paper [6], where the editor of the Journal of Solid State Circuits, L. Terman, solicited the preparation of a full paper which was later published in a Special Issue on Memories of the Journal of Solid State Circuits, [7].

To reduce the area required for implementation of capacitor pull-up circuitry as well as to improve the electrical performance of the logic circuitry, a modified two-level polysilicon-gate process was formulated. The modification included the use of two novel substructures. One of these substructures was a polysilicon-to-polysilicon
capacitor built on top of the field oxide and intended to substitute for the varactor used in the standard silicon-gate n-channel process. The other substructure was a novel way of implementing the MOST source and drain diffusions by diffusing through a polysilicon layer into the substrate. This polysilicon layer hence acts as a contact to the drain and source and serves as an additional interconnection level besides acting as a diffusion source for the MOST source and drain. This process was reported in the author's Ph.D. Thesis proposal, together with preliminary experimental results, and submitted in July 1975. A correspondence letter [10] in the May 1976 issue of the IEEE Transactions of Electron Devices by Middlehoek and Kooy has subsequently briefly explained the successful use of polysilicon-to-silicon contacts as well as the use of polysilicon as a diffusion source for the MOST source and drain.

Using the modified process and larger tolerances than is standard, 2-Ø, 3-Ø and 4-Ø shift registers and various test devices were designed and fabricated at the Carleton laboratories. The fabrication exercise showed that the modified process was indeed feasible, and provided valuable experimental information on the substructures. Computer simulation results for 2-Ø, 3-Ø and 4-Ø one-bit delays were performed and the results showed improvements in propagation delay, in high frequency performance, inverter power dissipation, and in the peak voltage levels representing logic ONES and ZEROS. Although the improvement in density was not great (20% less than the area required for the Small-Area Device), it was shown that if industrial tolerances were used, the corresponding inverter area reduction would be greater than 50%.
Possible applications of capacitor pull-up logic for use as shift registers and peripheral support circuits on larger LSI circuits were discussed. The propagation delay, power dissipation and area of the capacitor pull-up inverter was compared to that of an $I^2L$ inverter. The results for the capacitor pull-up inverter designed with the modified process showed a large improvement in the power-delay characteristics at higher frequencies. Further improvement is anticipated if the circuit were redesigned with standard industrial tolerances.

Although the use of capacitor pull-up circuitry with overlapping clocks was extensively investigated and reported, the topic has by no means been exhausted. The high frequency operation of these devices could be investigated further. Experimental work on devices fabricated with a double-level silicon-gate process would be of interest. This process does not necessarily have to be the same as discussed in Chapter 4. Use of local oxidation and VMOS processing may be considered both for improving electrical performance and for reduction in area required for circuit implementation.

The low frequency performance of capacitor pull-up circuits has not been investigated. Such circuits might find application where power consumption is a problem. At frequencies of the order of 1 kHz, the power dissipation is expected to be no greater than 1 nW per inverter.

Another area of investigation is the use of sine-wave operation instead of clock pulses. Investigations of the use of sine waves of low amplitude and very high frequency operating with a dc bias on devices of low threshold voltages ($\leq 0.1$ V) are of particular importance.
In a static logic, the power required to drive the circuitry is derived directly from the dc power supply. In a dynamic logic system however, the dc supply powers a static logic circuit, which derives the clock pulse waveforms necessary to drive the dynamic logic. Hence, a hypothetical system equation can be stated as follows:

\[(\text{Static logic}) = (\text{Dynamic logic}) + (\text{Static peripheral clocks})\]

It now becomes obvious that dynamic logic is ultimately limited in speed by the peripheral clock circuitry. For a large dynamic logic system, the capacitance loading on the clocks may be too large for them to derive the short rise times and fall times necessary for high frequency operation. In Table 6.1 of Chapter 6, it was stated that the capacitor pull-up inverter was expected to operate at frequencies of 80 MHz. For practical applications at this frequency, the rise time and fall time must be of the order of 1 ns. If it is not possible to design clocks that can derive clock pulse heights with the required rise time and fall time, then this poses the question as to whether it is at all necessary to have dynamic logic capable of high operational frequencies. Clocks derived externally to the package are not considered because they increase the package count, reduce the circuit gate-to-pin ratio and increase the power dissipation because they have to drive the parasitic 'can' capacitances. It is therefore of interest to research the limitations imposed on dynamic logic because of the necessity to derive clocks on chip.

The results presented in this thesis showed that capacitor pull-up circuits using overlapping clock pulses are capable of operating
at higher frequencies than other MOS dynamic circuits and that they dissipate less power in doing so. The problem of charge injection into the substrate as well as large inverter area caused by charge-sharing in the circuit of Crawford and Bazin were overcome. Experimental demonstration of circuit performance to 34.5 MHz was given and much higher frequency of operation was shown possible by simple computer extrapolation assuming the modified process which was developed in this thesis. The modified capacitor pull-up process was shown to reduce the area of capacitor pull-up circuitry to the point where it was comparable to other dynamic MOS, LSI circuitry.

The applications context for capacitor pull-up circuitry was discussed. Because of the inherent inability of the capacitor pull-up inverter to drive large capacitive loads, the circuit will find its best application in local high speed circuitry on chip, such as for multiplexing or development of high speed timing voltages. Therefore, the circuit is not inherently suitable for directly interfacing off chip.

The purpose of this was to carry forward the development of the circuit and process technology of the capacitor pull-up circuitry to the point where the potential advantages of speed and simplicity of operation could be realized. This purpose was achieved. Philosophically a very important and fundamental conclusion that can be made as a result of this research is that the normal sequence of a precharge followed by a conditional discharge to ground found in more common MOS dynamic logic circuits severely limits the high frequency performance of such circuits. Capacitor pull-up circuitry overcomes this by substituting a single
discharge to ground for the more common mode of operation. During the presentation of the conference paper [6], this point was of particular interest to those present. The capacitor pull-up technique serves to remind us that the way dynamic logic is being implemented at present may not be the best way possible.
REFERENCES


25. Emulsitone Company, Process Instructions, Form 03-03.


33. Private Communication with Dr. S.D. Rosenbaum and Dr. C.H. Chan, July 1976.


APPENDIX I

The model of the capacitor pull-up inverter that was discussed in Chapter 2 and in Chapter 4 did not consider the details of the MOST model since these were incorporated in the Nansim model. Figure A1.1(a) shows the inverter model, with the MOST gate OFF, and includes the parasitic gate-to-drain capacitance, $C_{gd}$. Figure A1.1(b) shows the inverter model with the driver MOST ON, for the case when the clock voltage on the capacitor $C_L$ is zero, the MOST is in the triode region. This represents the condition of the pull-up inverter when the output pulse to be developed is to represent a logic ZERO and just prior to application of the clock voltage to the top electrode of $C_L$. The MOST channel region is modelled by a distributed RC network. $(C_{g1}, C_{g2}, \ldots, C_{gn})$ and $(C_{d1}, C_{d2}, \ldots, C_{d(n-1)})$ represent the distributed value of the gate-oxide capacitance and the channel-depletion capacitance respectively. $(r_1, r_2, \ldots, r_{(n+1)})$ represent the distributed values of the channel ON-resistance.

When calculations of the output capacitance, $C_0$, were made for the 10-bit Large-Area Device and 16-bit Small-Area Device in Chapter 2, the contribution of the MOST to the output capacitor, $C_0$, say $C_X$, was neglected. This was done because the values of the load capacitor $C_L$, the drain diffusion junction capacitance $C_d$, and the other parasitic capacitances, such as $C_j$ and $C_{FINV}$ in Figure 4.1 of Chapter 4, are much larger than $C_X$. Hence, the capacitor divider ratio $(C_L/(C_L + C_0))$ was not significantly altered by neglecting $C_X$. 
Figure A1.1. (a) The figure shows the inverter model for the more optimum double-level polysilicon-gate n-channel capacitor pull-up inverter. $C_{gd}$ is the parasitic gate-to-drain overlap capacitance, and $C_d$ is the drain diffusion junction capacitance. $V_{in}=0$ V.

(b) The figure shows the inverter model for the case when the input gate is ON, i.e. $V_{in} \gg V_T$, and $V_{th}=0$ V. $(C_{g1}, C_{g2}, \ldots, C_{gn})$, $(C_{d1}, C_{d2}, \ldots, C_{d(n-1)})$, and $(r_1, r_2, \ldots, r_{(n+1)})$ are the distributed values of the gate-oxide capacitance, the channel-depletion region capacitance and the channel ON-resistance.

In each case, $C_L$, $C_{FO}$ and $C_D$ are as described in Chapter 4, Figure 4.1.
Figure A1.2. Schematic of inverter model used to calculate 
\((C_L/(C_L+C_0))\) at 0 V for the case when the MOST 
is 'ON' and \(V_P=0\) V.

For the modified two-level silicon-gate process, the values of 
the capacitors were reduced to a point where the contribution of the 
MOST, \(C_X\), could no longer be neglected if the MOST was ON. Because 
it is impossible to calculate \(C_X\) exactly due to its non-linear nature 
and due to the distributed nature of the channel region, it was arbitrarily 
decided to sum all the parallel capacitances \((C_{d1, \ldots, d(n-1)})\) 
to the drain-diffusion junction capacitance, \(C_d\). The effects of the 
capacitors \((C_{g1, \ldots, g_n})\) are neglected as are the distributed channel 
resistances \((r_1, r_2, \ldots, r_{(n+1)})\). The approximation to the capacitor 
pull-up model for the driver MOST ON is shown in Figure A1.2 and was 
used to calculate the capacitive divider ratio, \((C_L/(C_L+C_0))\) at 0 V, 
which was given in Table 5.4.

It should be noted that, because of the increased output capacitance, \(C_0\), when the MOST is ON, then the peak voltage level that is
developed for a logic ZERO, $V_{p0}$, is less than the peak voltage level for a logic ONE, $V_{p1}$. 