60 GHz System-on-Package Frequency Synthesizer
and Phase Lock Loop Optimization

by

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ABSTRACT

A 60 GHz synthesizer has been designed and manufactured using a Miniature Hybrid Microwave Integrated Circuit (MHMIC) packaging process developed at Communications Research Centre (CRC) of Canada, with FR4 PCB motherboard. The debugging and measurement work is performed on the synthesizer and the resulting phase noise is better than the derived requirements. The measured phase noise is -111.5 dBc/Hz (at 1 MHz offset) corresponding to an integrated phase noise of 2.8° at 57.6 GHz, resulting in a SNR degradation of only 1.8 dB.

A generic 3rd order PLL loop filter optimization procedure is presented for various VCO phase noise slopes, and C2/C1 capacitor ratios. The effect of the PLL loop filter resistor on the overall phase noise is investigated and a design procedure is presented for optimal design of a PLL loop filter.

The integrated phase noise specification is derived from system analysis to be 4°. The derivation process accounts for the effects of phase noise on OFDM, and ECC of the IEEE 802.15.3c standard. Various simulations are performed in Matlab and Simulink to verify that LDPC coding used in the standard brings the required SNR value to 1 dB from the Shannon limit.

A procedure is developed to derive the noise specification of the VCO and reference power supply in order to minimize its effect on the overall phase noise. The noise specification is derived for the selected VCO and reference.
ACKNOWLEDGEMENTS

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I am very thankful to my co-supervisor, Rony Amaya who guided my research at the Communications Research Center and helped me greatly with publications by always being there for me when a deadline is near, and investing a lot of his time to help me. Rony Amaya inspired me towards research in new and exciting areas, such as high power Gallium Nitrate devices, MEMS switches and varactors, mm-Wave synthesis, and many others.

I would also like to acknowledge the support of Communications Research Centre of Canada for fabrication, assembly, and testing of the synthesizer. Specifically, I would like to give my great appreciation to Adrian Momciu who worked with me at CRC and helped me greatly with manufacturing and testing. I would also like to thank Rob James for help with MHMIC fabrication, and Ibrahim Haroun for his help reviewing the research paper.
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<th>Description</th>
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<tr>
<td>ADI</td>
<td>Analog Devices Inc.</td>
</tr>
<tr>
<td>AWGN</td>
<td>Additive White Gaussian Noise</td>
</tr>
<tr>
<td>BER</td>
<td>Bit Error Rate</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complimentary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>COTS</td>
<td>Commercial Of-The-Shelf</td>
</tr>
<tr>
<td>CP</td>
<td>Charge Pump</td>
</tr>
<tr>
<td>CRC</td>
<td>Communications Research Centre of Canada</td>
</tr>
<tr>
<td>ECC</td>
<td>Error Control Coding</td>
</tr>
<tr>
<td>EIRP</td>
<td>Equivalent Isotropically Radiated Power</td>
</tr>
<tr>
<td>FCC</td>
<td>Federal Communications Commission (of the US)</td>
</tr>
<tr>
<td>GaAs</td>
<td>Gallium Arsenide semiconductor</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium Nitride semiconductor</td>
</tr>
<tr>
<td>Gbps</td>
<td>Giga bits per second</td>
</tr>
<tr>
<td>HD</td>
<td>High Definition</td>
</tr>
<tr>
<td>HDMI</td>
<td>High Definition Multimedia Interface</td>
</tr>
<tr>
<td>HSI</td>
<td>High Speed Interface (mode of 802.15.3c)</td>
</tr>
<tr>
<td>ICI</td>
<td>Inter-Carrier Interference (in OFDM)</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>ISI</td>
<td>Inter-Symbol Interference</td>
</tr>
<tr>
<td>ISM</td>
<td>Industrial, Scientific, and Medical band of electromagnetic spectrum</td>
</tr>
<tr>
<td>LDPC</td>
<td>Low Density Parity Check (coding)</td>
</tr>
<tr>
<td>LF</td>
<td>Loop Filter (for PLL)</td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator (a mixer port)</td>
</tr>
<tr>
<td>LOS</td>
<td>Line Of Sight</td>
</tr>
</tbody>
</table>
MCU  Micro-Controller Unit  
MHMIC  Miniature Hybrid Microwave Integrated Circuit  
NF  Noise Figure  
OFDM  Orthogonal Frequency Division Multiplexing  
P2P  Point-to-Point radio  
PA  Power Amplifier  
PAPR  Peak to Average Power Ratio  
PCB  Printed Circuit Board  
PFD  Phase-Frequency Detector  
PHY  Physical layer  
PL  Path Loss  
PPL  Phase Lock Loop  
PN  Phase Noise  
QAM  Quadrature Amplitude Modulation  
QPSK  Quadrature Phase Shift Keying  
RF  Radio Frequency  
RMS  Root Mean Square  
RRC  Root-Raised Cosine  
SC  Single Carrier (modulation)  
SiGe  Silicon Germanium semiconductor  
SNR  Signal to Noise Ratio  
SOC  System On Chip  
SOP  System On Package  
SSA  Signal Source Analyzer  
USB  Universal Serial Bus  
VCO  Voltage Controlled Oscillator  
Vt  Tuning voltage contact of a VCO  
WPAN  Wireless Personal Area Network  
XO  Crystal Oscillator
Chapter 1. **INTRODUCTION**

1.1 **MOTIVATION**

The advancement of processing power in mobile devices and the demand for high definition (HD) video streaming, as well as other high-data-rate transmission applications in the range of multi-Gigabits/sec, necessitates the use of the 60 GHz unlicensed ISM band (57-64 GHz). The main reason for the interest in the 60 GHz ISM band is attributed to the availability of 7-GHz of unlicensed bandwidth, which enables high data-rate transmission. Furthermore, the high Oxygen absorption around 60 GHz (Figure 1-1) makes this band well suited for frequency reuse, which increases the overall capacity. In addition, due to the high gain antennas required to overcome the path loss, harmful co-channel interference is minimized, and security of the communication is improved.

![Figure 1-1. Atmospheric Attenuation for Water Vapor and Oxygen [1].](image-url)
From Figure 1-1 we can see that, at 60 GHz, atmospheric Oxygen absorption is around 15 dB/km at sea level. The high attenuation is the reason why this band was not licensed before, as the gain of antennas has to be much higher compared to the other bands [2]. Now that most of the spectrum is congested below 60 GHz, and due to advancements in mm-Wave technologies, the 60 GHz band has become a commercially viable portion of spectrum for many telecommunications companies. Currently, there are many commercial applications available for 60 GHz that require high data rate transmission. Although the 60 GHz band is presently used, in limited capacity, for outdoor Point-to-Point communication where high bandwidth and unlicensed operation is desired (such as uncompressed video) the main future application of the band is in closed environments like office or home [3].

1.2 APPLICATIONS OF THE 60 GHz BAND

Very high data rate, short distance use of 60 GHz band creates new market segments. There are four main application areas where 60 GHz systems have a great value [2][3]: WPANs, Wireless HDMI, Kiosk, and Wireless Point to Point links, as shown:
Figure 1-2. Applications of 60 GHz Band.
1.2.1 WIRELESS HDMI

The use of the 60 GHz band for Wireless HDMI alleviates the need for the HDMI cable between TV and media storage, allowing flexibility in placement of the TV and increasing the esthetic appeal. For the Wireless HDMI to be truly useful and to replace current wired version, the system should be designed for non-LOS applications (eg. when media center is in a cabinet). The Wireless HDMI environment would most likely be single path propagation, with transmission distance of less than 10 m. For uncompressed full-HD video transmission the data rates would be around 2 Gbps [2].

1.2.2 POINT-TO-POINT LINKS

Telecommunication companies use a network of cellular towers to transfer data such as wireless internet and cell phone traffic between the consumer and telephone/IP networks. Aside from providing links between the towers and consumers, the towers contain multiple Point-to-Point (P2P) links, which transfer data between the towers. As the demand for wireless data rates increases (due to video-on-demand services) there is also a need to increase the capacity of these links. Due to spectrum congestion, and licensing fees, 60 GHz band offers significant cost savings. Unfortunately, the scale of implementation of 60 GHz P2P is limited by high atmospheric attenuation, to overcome which very high gain antennas are required (offsetting reduced costs due to no licensing). The typical communication range is between 100 m and 1 km. The data rates could be on order of 10’s of Gbps per link.

1.2.3 WPANs

The present WPANs use 2.4 GHz and 5.7 GHz ISM bands. The maximum reported data rates being on order of 1Gbps with distances in range of few dozen meters. The 60 GHz band offers data rates of up to 10’s of Gbps but for shorter (<10 m) distances confined to single room indoor usage. Therefore it is not able to completely replace present WPAN systems but rather augments them for short distance applications. These
applications include areas where USB, Firewire and other short range wired solutions are used, but, adding convenience, esthetics and high data rates.

1.3 60 GHz Standards

There are presently five standards that utilize the 60 GHz band: 802.11ad, 802.15.3c, WiGig, ECMA-387, and WirelessHD. The following table summarizes the PHY properties of these standards for maximum data rate per channel.

<table>
<thead>
<tr>
<th>Standard</th>
<th>Max data-rate, Gbps</th>
<th>Max data-rate modulation</th>
<th>Release date</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEEE 802.15.3c</td>
<td>5.775</td>
<td>64-QAM OFDM, code rate 5/8</td>
<td>Sept 2009</td>
<td>Public</td>
</tr>
<tr>
<td>IEEE 802.11ad</td>
<td>6.757</td>
<td>64-QAM OFDM, code rate 13/16</td>
<td>~ Dec 2012</td>
<td>N/A</td>
</tr>
<tr>
<td>WiGig</td>
<td>6.757</td>
<td>64-QAM OFDM, code rate 13/16</td>
<td>Dec 2009</td>
<td>Private</td>
</tr>
<tr>
<td>ECMA-387</td>
<td>6.35</td>
<td>16-QAM, no coding</td>
<td>Dec 2008</td>
<td>Public</td>
</tr>
<tr>
<td>WirelessHD</td>
<td>7.138</td>
<td>64-QAM OFDM, code rate 5/6</td>
<td>May 2010</td>
<td>Public*</td>
</tr>
</tbody>
</table>

* Summary only, access to full specification requires registration

IEEE 802.15.3c is chosen for the thesis due to its large constellation size for worst case phase noise degradation and public availability of the specification at the time of the design. Additionally, there is significantly more results being reported on the use of this standard compared to others. The IEEE 802.15.3c standard has two modes of operation: single carrier (SC) and multi-carrier (HSI) that uses OFDM. Next, a list of various modulation schemes for HSI mode is presented:
Table 1-2. HSI Modes of IEEE 802.15.3c.

<table>
<thead>
<tr>
<th>MCS Index</th>
<th>Data rate (Mb/s)</th>
<th>Modulation Scheme</th>
<th>ECC rate msb 8b</th>
<th>Isb 8b</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>32.1</td>
<td>QPSK</td>
<td>1/2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1540</td>
<td>QPSK</td>
<td>1/2</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>2310</td>
<td>QPSK</td>
<td>3/4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>2695</td>
<td>QPSK</td>
<td>7/8</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>3080</td>
<td>16-QAM</td>
<td>1/2</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>4620</td>
<td>16-QAM</td>
<td>3/4</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>5390</td>
<td>16-QAM</td>
<td>7/8</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>5775</td>
<td>64-QAM</td>
<td>5/8</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>1925</td>
<td>QPSK</td>
<td>1/2</td>
<td>3/4</td>
</tr>
<tr>
<td>9</td>
<td>2503</td>
<td>QPSK</td>
<td>3/4</td>
<td>7/8</td>
</tr>
<tr>
<td>10</td>
<td>3850</td>
<td>16-QAM</td>
<td>1/2</td>
<td>3/4</td>
</tr>
<tr>
<td>11</td>
<td>5005</td>
<td>16-QAM</td>
<td>3/4</td>
<td>7/8</td>
</tr>
</tbody>
</table>

The highest data rate mode uses 64-QAM and 5/8 code rate providing data rate of 5.775 Gbps. This particular mode uses a Low-Density Parity Check (LDPC) Error Correction Coding (ECC) to provide error tolerance against additive noise at expense of reduced data rate. Since this mode uses the highest density constellation and highest data rate it will be adopted here for the design of the synthesizer.

1.4 CHALLENGES

Although the 60-GHz band has many advantages, the design of low-cost high-performance frequency synthesizers that meet the system requirements of low phase noise presents a design challenge, particularly, when CMOS system-on-chip (SOC) is the technology to be used. Such challenges are mainly due to the lossy silicon-substrate present in CMOS technologies. This is the main reason for using GaAs-based COTS components in this work. The advantage of SOP integration is that, it enables the realization of the passive components on the same substrate of the package as the active
components, minimizing interconnection losses and improving overall cost. In addition, active devices can be selected from different technologies to optimize the system performance. As an example, CMOS components can be used for high-density logic and analog circuits, SiGe and GaAs for high speed microwave circuits, and GaN for high power [8].

1.5 THESIS CONTRIBUTIONS

• A connectorized 60 GHz synthesizer with the lowest measured integrated phase noise across published SOP and SOC state of the art synthesizers and transceiver systems.

• Generalized 3rd order PLL Loop Filter optimization procedure for minimization of integrated overall phase noise of a PLL. Previous published works never considered, in general form, the phase noise contributions from the Reference and/or the Voltage Controlled Oscillator (VCO). Previous reported results were either specific to the standard or didn’t use the Reference or the VCO phase noise.

• Derivation of phase noise specification for the IEEE 802.15.3c radio based on path loss SNR and peak power FCC requirements. Based on the background research, this was never done for ECC coded signal using this standard. Furthermore, this work presents a set of ready-to-use plots of SNR degradation vs. phase noise requirement for 802.15.3c modulations schemes, which is very useful for any one designing a 802.15.3c radio system.

• Derivation of power supply noise specification based on tolerable phase noise degradation for VCO and Reference Oscillator.

• Submitted a paper based on this work to IEEE Custom Integrated Circuits Conference (2011).
1.6 **Thesis Organization**

Chapter 2 gives background information on the concepts used in further chapters, such as digital modulation, Shannon channel capacity, phase noise and its effect on OFDM, and Phase Lock Loops. Chapter 3 contains a system-level analysis of an 802.15.3c radio for the derivation of phase noise specification. The system analysis considers FCC requirements, path loss, Error Control Coding, and phase noise effects on OFDM. Minimum phase noise and SNR requirements are derived based on a specific radio setup, but the process described in the chapter can be used for any path loss or phase noise.

Synthesizer design is presented in Chapter 4, starting with critical component selection. A generic 3rd order PLL loop filter phase noise optimization procedure is followed with useful design plots for arbitrary VCO phase noise slope. Then, a power supply noise requirement is derived and applied to the design of voltage regulators for the VCO and the reference crystal oscillator. Implementation of the synthesizer is presented in Chapter 5. The chapter starts with an introduction to the MHMIC packaging process, followed by a detailed thermal analysis, and concludes with the MHMIC layout. In Chapter 6 the PCB packaging and layout are described. Chapter 7 presents the measurement setup and measurement results with a discussion of the measured results and comparison to the simulation. Final Chapter 8, summarizes the work, highlighting the results and thesis contributions, and makes suggestions for future synthesizer improvements.
Chapter 2. BACKGROUND THEORY

The following sections will introduce key concepts that are used in later chapters: basics of digital modulation, Shannon channel capacity, phase noise and its effect on OFDM, and background on Phase Lock Loops.

2.1 DIGITAL MODULATION

Due to the digital revolution at the end of 20th century, most of the communication standards have been converted from analog to digital. Modern communication systems commonly utilize both amplitude and phase of a signal to carry information, with phase and amplitude taking pre-defined discrete values [9]. Unfortunately, creating abrupt changes in phase or amplitude, by using rectangular pulses, creates significant spectral leakage. This is due to sin(x)/x spectrum of rectangular pulse-shaped data. Because of this inefficient use of spectrum the signal must be passed through a pulse-shaping filter, such as a commonly used, Root-Raised Cosine (RRC) filter. The advantage of RRC filter is that it is also used at the receiver (matched filter) resulting in a raised cosine response, which satisfies the Nyquist criteria for zero Inter-Symbol-Interference (ISI) [10].

The phase encoding can be done either by directly modulating the phase of the sine-wave or by decomposing the modulation into orthogonal components (sine and cosine) which are combined at a later stage (typically at non-zero center frequency). Digitally combining at non-zero frequency allows removal of the image in digital domain, with very large image rejection ratios. Large rejection ratios allows utilization of cheaper output filters for LO rejection, and reduced requirements for power amplifier linearity.

Because both, sine and cosine, are modulated separately the combined signal can be represented on a complex plane. After applying the matched filter (to get zero ISI) and mixing down to zero IF one can plot the received signal on a complex plane with the resulting plot referred to as constellation. For example, Figure 2-1 presents the
constellation diagram for 64-QAM (8x8, or 3 bits for phase and 3 bits for amplitude) with Signal to Noise Ratio (SNR) of 30 dB and its spectrum:

Figure 2-1. 64-QAM Constellation and its Spectrum.

2.2 **SHANNON CHANNEL CAPACITY**

In order to know the required Signal to Noise Ratio (SNR) for 802.15.3c modes of operation first we can determine the minimum possible SNR required, which can be found using the Shannon channel capacity theorem. Shannon theorem states that given the SNR and available bandwidth there is a maxim obtainable bit rate for signal in Additive White Gaussian Noise (AWGN) channel with arbitrary small amount of errors. According to Shannon [11] the maximum data rate, called the channel capacity, can be calculated as follows:

\[ C = B \log_2 (1 + S/N) \]  (2.2.1)

Where \( C \) is data rate in bits/s, \( B \) is bandwidth in Hz, and \( S/N \) corresponds to the SNR in bandwidth \( B \). For MxM QAM the bit rate is \( C = 2B \log_2 (M) \) for complex signals [11] [12]. To reach Shannon capacity the signal must be passed through error correction coding which adds extra data bits for error correction. The result is that total data consist
of useful data plus extra, therefore effective data rate is reduced. This reduction in data rate is quantified by a code rate, \( r \), for example \( r=5/6 \) code rate means there out of every 6 bits there is 5 bits of data and 1 bit extra. Reversing equation (2.2.1) we can derive the minimum required SNR to achieve no-error transmission given the data rate that we require, constellation size, and code rate:

\[
SNR_{\text{min}} = 10 \cdot \log_{10}(2^{rM} - 1)
\]  

(2.2.2)

This equation will be used later to derive the minimum required SNR values for different modes of 802.15.3c.

### 2.3 OFDM

As seen in Figure 2-1, even with RRC pulse shaping, the QAM spectrum has a large spectral leakage beyond its Nyquist frequency bandwidth, corresponding to \( \frac{1}{2} \) of the sampling frequency. In many situations this would require additional filtering to meet spurious emission requirements of particular standard. Another approach is to make signal spectrum more rectangular, and therefore more spectrally efficient, allowing signal spectrum come closer to the adjacent channels, utilizing more of the allocated spectrum. Due to the \( \sin(x)/x \) frequency roll-off, the spectral regrowth decays proportionally to the data rate (higher data rate - more excess bandwidth), allowing for the use of multiple smaller data rate signals which can be later combined to minimize ISI. The result is Orthogonal Frequency Division Multiplexing (OFDM). OFDM relies on the fact that the same-data-rate signals spaced at the symbol rate will not interfere with each other [13], as can be shown through Nyquist theorem for no ISI. Figure 2-2 illustrates how an OFDM spectrum is produced by a combination of subcarriers and the resulting spectrum.
Although OFDM is a lot more spectrally efficient than single carrier (SC) schemes [13], there are many disadvantages as well. Due to the orthogonality of the subcarriers there are times when all the subcarriers have a high amplitude which leads to very high peaks, causing the signal to have a high Peak to Average Power Ratio (PAPR). This is problematic for linearity requirement of the power amplifier and will be discussed in Chapter 3. Another major difficulty with OFDM is that, if one subcarrier is moved it creates an Inter Carrier Interference (ICI) across all other subcarriers [14][15]. This effect can be caused by phase noise in the local oscillator or digital clock which causes random movement of the subcarriers. This is explained in greater detail in next section.
2.4 Phase Noise

Phase noise can be represented as a phase modulating signal of a sine wave [16]:

\[ V(t) = A \cdot \sin(\omega_c t + \phi_n(t)) \]  

(2.4.1)

If phase noise is relatively small, which is usually the case for properly designed system, \( \phi_n(t) \) can be removed out of the sine using trigonometric identities:

\[ V(t) = A(\cos(\omega_c t) - \sin(\omega_c t) \cdot \phi_n(t)) \]  

(2.4.2)

Noting that the signal has two portions, the original signal and phase modulated one, we can further express \( \phi_n(t) \) as a Fourier series with a frequency variable \( \omega_m \) (offset frequency). Dividing the power of the phase noise by the signal power we get a carrier-relative spectral density of the phase noise which can be expressed as [16]:

\[ PN_{DSB, dB}(\omega_m) = 10\log_{10} \left( \frac{\phi_{rms}^2(\omega_m)}{R} \right) \quad [dBc/Hz] \]  

(2.4.3)

The phase noise modulation is graphically expressed as a spectral density distribution:

```
Figure 2-3. Phase Noise Spectrum of a Single Tone.
```

Applying phase noise to an OFDM signal would create a very complicated situation, as the subcarrier frequencies are orthogonal, any phase change of even one subcarrier
breaks the orthogonality. And when adding them all together the phase noise relationship between subcarriers becomes very complex [15][17]. This makes the phase noise add up across all the subcarriers, which is in contrast to single carrier modulation. The mathematical details of this are investigated in Chapter 3. Below is a plot illustrating the effect of phase noise of one of the subcarrier to others:

![Figure 2-4. OFDM with Degraded Orthogonality due to Phase Noise.](image)

### 2.5 Phase Lock Loops

In order to generate a signal in the 60 GHz band we need to upconvert the signal from an Intermediate Frequency (IF) to the desired radio frequency (RF). Using a single upconversion and given the IF frequency the LO frequency is just RF – IF. Were RF frequency is centered at one of the channels of 802.15.3c:

<table>
<thead>
<tr>
<th>CHNL_ID</th>
<th>Start frequency(^a)</th>
<th>Center frequency</th>
<th>Stop frequency(^a)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>57 240 GHz</td>
<td>58 320 GHz</td>
<td>59 400 GHz</td>
</tr>
<tr>
<td>2</td>
<td>59 000 GHz</td>
<td>60 480 GHz</td>
<td>61 560 GHz</td>
</tr>
<tr>
<td>3</td>
<td>61 560 GHz</td>
<td>63 040 GHz</td>
<td>64 520 GHz</td>
</tr>
<tr>
<td>4</td>
<td>63 820 GHz</td>
<td>65 800 GHz</td>
<td>65 880 GHz</td>
</tr>
</tbody>
</table>
The LO frequency has to be tunable such that the RF frequency can be changed to any of these channels (Table 2-1). A transmitter and a receiver must have the same LO frequency in order to recover the data without errors. The accuracy and phase noise has to be good enough for the digital demodulator to work properly [8]. The phase noise can be minimized by design if the required maximum allowable value can be determined, which is performed in Chapter 3. The frequency accuracy can be guaranteed by locking transmitter and receiver LOs to their respective stable Crystal Oscillators (XOs). This function is typically performed by locking a high frequency VCO to a lower (Reference) frequency with a Phase Lock Loop (PLL).

A typical modern PLL includes a digital Phase Frequency Detector (PFD), Charge Pump (CP), VCO, Loop Filter (LF), N and R dividers, and a reference oscillator [18][19][20]:

![Phase Lock Loop Block Diagram](image)

Figure 2-5. Phase Lock Loop Block Diagram.

The loop works by comparing the phase and frequency of the VCO and the reference and adjusting the VCO tuning voltage such that the frequency of reference and VCO are multiple of each other \(f_{\text{VCO}}=N/R\cdot f_{\text{REF}}\). The phase noise of the XO reference is also multiplied by \(N/R\) due to the upconversion in frequency.
Reference phase noise is filtered out by the LF, such that the added overall phase noise is minimized (see Section 4.5). At higher offset frequencies the loop filter diminishes the influence of the reference phase noise on the overall phase noise, allowing for the VCO phase noise to dominate. The resultant phase noise response can be separated into in-band and out-of-band portions as shown on Figure 2-6.

![Figure 2-6. PLL Phase Noise.](image)

Now that all main concepts are described, the synthesizer design can begin. But first a system analysis is performed in the following chapter in order to come up with the phase noise requirement for the synthesizer.
Chapter 3. SYSTEM ANALYSIS

3.1 THE SNR REQUIREMENT

Before presenting the analysis and design of the synthesizer we need to understand the transceiver as a system, so it is clear how the synthesizer affects system performance. The following sections will describe how the SNR of the system is derived from a top level specifications and how the SNR is degraded by the phase noise of the synthesizer. The model presented here begins with an ideal case and builds on the non-idealities of various system components and the effect each have on the degradation of SNR. This work starts by presenting the system’s link budget, followed by the SNR derivation based on the peak power requirement, then by the phase noise degradation of SNR, and finally by the effect of Error Control Coding (ECC) on the SNR requirement. At which point the phase noise specification is finalized in light of improved SNR due to the ECC.

3.1.1 SYSTEM OVERVIEW

In order to begin deriving the system and synthesizer specification a radio architecture must be defined first. The choice of a particular radio architecture affects the synthesizer frequency range and channel spacing specification and therefore needs to be selected first. For simplicity, and to test the synthesizer at the highest possible frequency, a simple superheterodyne [8], single frequency conversion, architecture is used. The experimental setup is presented in Figure 3-1, and is designed to test downstream transmission in the 60 GHz range. For simplicity, this particular implementation takes several channels from IEEE 802.11n (5.5 GHz) signal and upconverts them to 60 GHz range. The purpose of the setup is to verify the system design and evaluate synthesizer performance at 60 GHz. Based on the specifications of commercially available VCOs, the synthesizer frequency
range would be 56 – 60 GHz but not all of it will be utilized as it is limited by the 802.15.3c high frequency limit of 65.8 GHz.

![Diagram of radio system](image)

Figure 3-1. Radio System in which Proposed Synthesizer would be used.

### 3.1.2 LINK BUDGET

Following the standard specifications of IEEE 802.15.3c [1] the required system specifications can be derived based on the proposed radio system. A standard process of radio system design requires knowledge of the environment in which the radio operates. The required Path Loss of the radio link determines the SNR and ultimately the Bit-Error-Rate (BER) of the system based on attenuation of the signal with distance. Based on the work of the members of the IEEE 802.15.3c task group [1][21] we define the system specifications in order to reduce the number of design variables:
Table 3-1. Summary of System Specifications

<table>
<thead>
<tr>
<th>Specification type</th>
<th>Specification Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard and modulation scheme</td>
<td>802.15.3c, HSI PHY mode index 7. 512-subcarrier 64-QAM OFDM with subcarrier frequency spacing of 5.15625 MHz</td>
</tr>
<tr>
<td>Distance</td>
<td>10 m (at BER=10^{-6}). Typical in-door scenario.</td>
</tr>
<tr>
<td>Antenna gain</td>
<td>8 dBi (TX), 24 dBi (RX), as used in [21]</td>
</tr>
<tr>
<td>Antenna parameters</td>
<td>Perfect co-polarization. LOS. Beam steering is assumed to achieve desired gain.</td>
</tr>
<tr>
<td>Channel Model</td>
<td>Rician fading channel based on [21] used in Path Loss. AWGN used in BER plots.</td>
</tr>
<tr>
<td>Transmit power</td>
<td>27 dBm EIRP average, 27 dBm peak (across 7 GHz) [22]</td>
</tr>
<tr>
<td>Receiver Noise Figure (NF)</td>
<td>6 dB (2 dB worse than the min. reported for 60 GHz applications [3])</td>
</tr>
<tr>
<td>Nominal used bandwidth</td>
<td>1.815 GHz (data + pilot tones)</td>
</tr>
<tr>
<td>PAPR reduction</td>
<td>No PAPR-reducing coding (worst case scenario)</td>
</tr>
</tbody>
</table>

The average Path Loss (PL) for multipath propagation is calculated as follows [21][23]:

\[
PL(d)_{dB} = PL_0 + 10 \cdot n \cdot \log_{10}\left(\frac{d}{d_0}\right) + S(d) \tag{3.1.1}
\]

Where \(d_0\) is reference distance, at which \(PL_0\) is measured, \(PL_0\) is PL in dB with antenna gains removed, \(n\) is the PL exponent, \(S(d)\) is a shadowing coefficient with zero mean standard deviation \(\sigma_s\). Using values for \(PL_0\), \(n\), \(d_0\), \(\sigma_s\) from [21]: \(PL_0=36.9\) dB, \(n=1.7\), \(d_0=1\) cm, \(\sigma_s=1.6\) which are derived from measurements in a residential LOS environment with high gain antennas. Using (3.1.1) for distance \(d\) of 10 m and shadowing loss of one \(\sigma_s\) \((S(d)=\sigma_s)\) the PL is \textbf{90.4 dB}. For comparison, Friis transmission equation [24] yields a PL of 88.2 dB. The small difference between Friis and (3.1.1) path loss calculations indicates that there is little multipath or shadowing.
The maximum attainable input power to the receiver is calculated as follows [24]:

\[ P_{r,\text{max}[dBm]} = EIRP_{\text{max}[dBm]} + G_{RX}[dB] - P_L[dB] \]  \hspace{1cm} (3.1.2)

Which gives maximum received power of -39.4 dBm for the transmit power of 19 dBm (27 dBm - 8 dBi). Then the maximum achievable SNR can be computed as follows [16]:

\[ SNR = P_r[dBm] + 174\frac{dBm}{Hz} - 10\log_{10}(BW_{Hz}) - NF_{RX} \]  \hspace{1cm} (3.1.3)

For a receiver with a NF of 6 dB the maximum obtainable SNR in full channel bandwidth of 1.815 GHz is 36 dB. This figure neglects antenna noise temperature, phase noise, non-linearity of the TX power amplifier (PA), and back-off required to meet peak TX power specification (27dBm) which is considered next.

### 3.1.3 Peak Power Requirement

Due to the multi-carrier nature of OFDM, it has a higher Peak to Average Power Ratio (PAPR) than a Single Carrier (SC) signal. With no PAPR-reduction, such as peak filtering or coding, the worst case PAPR can be calculated as a function of number of active sub-carriers [14]:

\[ PAPR_{dB} = 10 \cdot \log_{10}(N) \]  \hspace{1cm} (3.1.4)

Where \(N\) corresponds to 336 (data) + 16 (pilots) = 352 (802.15.3c HSI mode), for which PAPR is 25.5 dB. This means that the average power would have to be 25.5 dB below the maximum 27 dBm peak power specified by FCC [22]. Therefore, if no PAPR reduction techniques are applied, the average transmit power would drop from 19 dBm (based on EIRP requirement) to 1.5 dBm, a 17.5 dB loss in transmit power due to peak
power constraint. SNR would also degrade by the same amount to 18.5 dB. Typically an improvement of at least 10 dB from PAPR can be achieved by peak filtering and coding [14]. For this improvement in PAPR, the maximally obtainable SNR, due to path loss, would be 28.5 dB (down from 36dB based on just EIRP requirement), and average output power of 11.5dBm.

3.2 PHASE NOISE EFFECT ON THE SNR

The probability of bit error for MxM QAM without Error Correction Coding (EEC) can be expressed as [25]:

\[ P_B \approx \frac{1}{M \log_2(M)} \cdot \text{erfc} \left( \sqrt{\frac{3 \cdot SNR}{2(M^2 - 1)}} \right) \quad (3.2.1) \]

According to [15] in a AWGN channel the SNR degradation due to phase noise in OFDM is independent of subcarrier spacing or number of subcarriers and can be calculated as follows:

\[ SNR_{with\, PN} = \frac{e^{-4\sigma_\phi^2}}{1 - e^{-4\sigma_\phi^2} + 1/ SNR_{without\, PN}} \quad (3.2.2) \]

Where \( \sigma_\phi \) corresponds to the phase noise variance in radians and which can be calculated by integration of the phase noise spectral density as follows:

\[ \sigma_\phi = \sqrt{2 \int_{f_{\text{min}}}^{f_{\text{max}}} S_\phi(f) \, df} \quad (3.2.3) \]
Where $S_{\phi}(f)$ is a single-sideband phase noise density (rad$^2$/Hz), and $f_{max}$ and $f_{min}$ are minimum and maximum offset frequencies where phase noise is significant.

The constellation on Figure 3-2 illustrates the effect of phase noise on the constellation for 64-QAM with $0^\circ$, $4^\circ$, and $6^\circ$ of integrated phase noise and 20 dB SNR:

Figure 3-2. 64QAM, 20dB SNR, and Phase Noise (left to right: $0^\circ$, $4^\circ$, $6^\circ$).

Figure 3-3 shows the result of a Matlab simulation using equation (3.2.2) for top data-rate modulation schemes of 802.15.3c (QPSK, 16-QAM, 64-QAM) and a commonly used BER values of: $10^{-3}$, $10^{-5}$, $10^{-6}$.
Figure 3-3. SNR Degradation from Phase Noise for Various BER’s ($10^{-3}$, $10^{-5}$, $10^{-6}$) and Modulation Schemes of 802.15.3c with no ECC.
As shown in the previous section, the SNR at maximum peak power (without phase noise) was found to be 28.5 dB. Considering the highest available data-rate scheme, 64QAM, and BER of $10^{-6}$ we can see that the required SNR for this BER would have to be 26.5dB (without phase noise). Therefore we have a 2 dB margin if we use the maximum peak power. This margin is further reduced if phase noise is added to the signal. The maximum allowable phase noise that can be tolerated at the max peak power while still achieving BER of $10^{-6}$ can be found by looking at Figure 3-3. At 2dB SNR degradation, the required maximum integrated phase noise cannot exceed 0.8 degrees. This value assumes no ECC and is revised in next section.

Figure 3-4 BER “Waterfall” Diagram Showing BER Degradation Caused by the Phase Noise based on equations (3.2.1) and (3.2.2). Phase Noise Variances: 0°, 0.5°, 1°, 1.5°, 2°. No ECC.
3.3 **Effect of Error Control Coding on Phase Noise Spec.**

Since ECC will significantly reduce the required SNR for a given BER, especially at high BERs, we need to look at the effect of SNR degradation due to phase noise at SNR levels achievable with ECC. According to the literature [26], Low-Density-Parity-Check (LDPC) coding can closely approach Shannon Limit (minimum SNR for arbitrary low probability of error). According to the Shannon theorem, recall from Chapter 2 – the minimum SNR for M×M QAM signal is:

\[
SNR_{\text{min}} = 10 \cdot \log_{10}(2^{r \cdot M} - 1)
\]  (3.3.1)

Where \( r \) is the code rate, and \( M \) is the constellation dimension (as in M×M QAM).

The reported SNR distance to Shannon Limit for LDPC encoded signal can reach 1 dB at relatively low probabilities of bit error (< 10\(^{-6}\)) [26]. For a given modulation scheme we can find out the Shannon Limit SNR, and considering that coding can bring the SNR to within 1 dB of Shannon Limit, we can look at how phase noise would influence ECC coded signal using equations (3.2.2) and (3.2.3). The Shannon limited SNR’s that can be achieved for different modulation schemes are presented in Table 3-2 for a case of AWGN (binary-unconstrained) channel:

**Table 3-2. Summary of Coding and Modulation Schemes.**

<table>
<thead>
<tr>
<th>802.15.3c MCS index</th>
<th>Modulation Scheme</th>
<th>Shannon Limit, SNR, dB</th>
<th>SNR used for PN calculations, dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>QPSK (r=1/2)</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>QPSK (r=3/4)</td>
<td>2.6</td>
<td>3.6</td>
</tr>
<tr>
<td>3</td>
<td>QPSK (r=7/8)</td>
<td>3.7</td>
<td>4.7</td>
</tr>
<tr>
<td>4</td>
<td>16-QAM (r=1/2)</td>
<td>4.8</td>
<td>5.8</td>
</tr>
<tr>
<td>5</td>
<td>16-QAM (r=3/4)</td>
<td>8.4</td>
<td>9.4</td>
</tr>
<tr>
<td>6</td>
<td>16-QAM (r=7/8)</td>
<td>10.1</td>
<td>11.1</td>
</tr>
<tr>
<td>7</td>
<td>64-QAM (r=5/8)</td>
<td>14.9</td>
<td>15.9</td>
</tr>
</tbody>
</table>
Using equations (3.2.2) and (3.2.3) for each modulation scheme and rate from Table 3-2 the plot on Figure 3-5 shows the SNR degradation due to the phase noise, assuming that the SNR is 1 dB from Shannon Limit.

![SNR Degradation due to Phase Noise](image)

Figure 3-5 SNR Degradation due to the Phase Noise for 802.15.3c Modes with SNR 1 dB from Shannon Limit.

Comparing the Shannon limit to results of Figure 3-5 and Figure 3-3 we can see that ECC desensitizes the system against phase noise. For example with a variance of $1^\circ$ the difference in SNR for 64-QAM is only 0.3 dB, compared to 3.5 dB for non encoded signal.

It can be noted from Figure 3-4 that the BER curves flatten for very high SNR, which means that if phase noise is higher than certain, to be defined, value, it’s impossible to
reduce error probability by increasing SNR. This BER limit and its dependence on modulation scheme and phase noise is show on Figure 3-6 for the case without ECC:

Figure 3-6 Best Achievable BER (infinite SNR) as a Function of the Phase Noise Variance and Modulation with no ECC.

The worst-case, LDPC (420,672) rate 5/8 coding (802.15.3c MCS index 7), is applied to the signal which is then 64-QAM modulated with Gray\textsuperscript{1} mapping. The signal is then passed through AWGN channel with variable SNR and then demodulated by 64-QAM log-likelyhood detector, and error-corrected by an LDPC decoder. The results of the BER performance of ECC coded and not coded 64-QAM signals are shown on Figure 3-7:

---

\textsuperscript{1} Gray mapping is a method, developed by Frank Gray, that assigns bit values to constellation points such that only 1 bit error occurs when there is noise that brings the signal across symbol decision boundary.
From Figure 3-7, above, we can see that for 64-QAM LDPC ECC achieves performance remarkably close to the Shannon Limit. The SNR at BER of $10^{-6}$ is 15.8 dB, only 0.9 dB away from Shannon Limit. This 15.8 dB SNR value is used in further analysis of the phase noise effect on SNR degradation.

At max peak power the best achievable SNR was previously found to be 28.5 dB (Section 3.1.3). The required SNR from Figure 3-7 is 15.8 dB (for BER of $10^{-6}$). Looking at Figure 3-5 this means that the system can tolerate 19° of phase noise variance and still achieve BER of $10^{-6}$ with 10 dB PAPR-reducing coding (average power limited), and 4°
without PAPR correction (peak power limited). In worst case scenario, with no PAPR coding the synthesizer need to provide at most 4° of integrated phase noise.

3.4 SYSTEM ANALYSIS SUMMARY

Worst case, 64-QAM OFDM, signal with LDPC(420,672) error correction and code rate of 5/8 is used for derivation of required SNR. The worst case SNR is derived, assuming no PAPR correction, to be 18.5 dB for 10 m link with BER of $10^{-6}$ and RX/TX antenna gains of 8 dBi and 24 dBi respectively. Phase noise specification is derived from simulation results and the integrated phase noise specification is shown to be 4°. If PAPR correction is used with integrated phase noise of 4° then the average TX power (and SNR) can be increased by 10dB, from 1.5dBm to 11.5dBm. This would allow distance to be increased from 10m to 38m (for the same SNR and BER). Alternatively, this can be also used to relax gain requirement of the antennas. The worst-case scenario is assumed and the synthesizer specification is fixed at 4° of integrated phase noise (in 1.815 GHz channel bandwidth). The Next chapter shows the design of the synthesizer that meets this requirement.
Chapter 4. **SYNTHESIZER DESIGN**

4.1 **PLL INTRODUCTION**

From previous chapter it was determined that we need at most 4° of the overall integrated phase noise and that a frequency synchronization source, such as a crystal oscillator (XO) would be required, so that the receiver and the transmitter LO frequencies are sufficiently close together. We also need the phase of transmit LO to be relatively steady [8], with respect to the receiver LO, otherwise the receiver demodulator will not be able (not fast enough) to recover proper phase of the received signal and will not sample the analog received signal at the right intervals introducing inter-symbol interference (ISI). Therefore, we need a frequency synthesizer in the receiver and the transmitter with both phase and frequency close enough to each other such that the receiver can track the phase variations introduced by the transmitter. To accomplish this, several commonly used approaches can be used, as described below:

**Table 4-1. Comparison of Frequency Synthesis Methods**

<table>
<thead>
<tr>
<th>Method of synthesis</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
</table>
| Phase Locked Loop (PLL)      | -Can optimize phase noise by adjusting the loop filter bandwidth  
|                               | -Can synthesize frequencies with arbitrary step size | -Higher phase noise at lower frequency offsets     |
| Multiply the reference       | -Low phase noise at lower offsets             | -High phase noise at higher frequency offsets      
|                               |                                               | -Practically can only synthesize single frequency |
| Injection-lock the oscillator| -Low phase noise at lower offsets             | -Can't control injection BW                       
|                               | -Lower phase noise than multiplier approach at higher frequency offsets | -Temperature, and power supply variation constrain oscillator to utilize lower Q resonator |
Since the IEEE 802.15.3c communication standard utilizes multiple channels (Table 1-1) the synthesizer must be able to generate frequencies with a specified step size of 2.16 GHz (Table 2-1). The only practical way to do this is with a PLL, as other approaches would be extremely bulky due to the required filter banks. Also, in terms of phase noise performance a PLL offers the best flexibility, at the expense of increased phase noise at low frequency offsets (in-band). If properly designed, the in-band phase noise degradation in the PLL can be minimized through accurate selection of the reference source, phase-frequency detector (PFD), dividers and the loop filter. The following sections will show the steps in this selection process and performance optimization following the selection.

4.2 PLL DESIGN

For simplicity and quicker turnaround a standard PLL topology is used with a PLL chip that contains PFD, R/N dividers, and CP. The component selection process is described in Section 4.3. The structure of the synthesizer is presented on Figure 4-1.
The proposed synthesizer uses commercial-of-the-shelf (COTS) components for the reference XO, dividers, phase-frequency detector (PFD), Op-Amp-based loop filter, VCO, x4 multiplier and final amplifier. The output filter and the synthesizer substrate are manufactured in an in-house Miniature Hybrid Microwave Integrated Circuit (MHMIC) process. For the particular 60 GHz test system, described in Chapter 3, the channel spacing is not very important, and a channel spacing of 3.2 GHz is chosen, based on 0.1 GHz reference, and PDF frequency. Frequency switching speed is also not critical.

Based on the 60 GHz mixer specifications the required power output has to be between 13 dBm and 20 dBm. Therefore the synthesizer is designed to provide at least 18
dBm power, due to the expected 3dB loss in LO filter, and simulated 3 dB of extra losses in bond-wires and transmission lines.

4.3 PLL COMPONENT SELECTION

The following components are selected based on simulation of their phase noise contributions and availability:

Table 4-2. Bill of Materials for Active Components.

<table>
<thead>
<tr>
<th>Type</th>
<th>Manufacturer P/N</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL chip (N/R dividers, PFD, CP)</td>
<td>ADF4106BCP</td>
<td>Analog Devices</td>
</tr>
<tr>
<td>VCO (14-15GHz) and 1/8 divider</td>
<td>HMC398QS16G</td>
<td>Hittite</td>
</tr>
<tr>
<td>x4 multiplier</td>
<td>HMC-XDH158</td>
<td>Hittite</td>
</tr>
<tr>
<td>Output Amplifier</td>
<td>HMC-ABH241</td>
<td>Hittite</td>
</tr>
<tr>
<td>Op-Amp</td>
<td>OPA2111DRGT</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>Crystal Oscillator (XO)</td>
<td>CVHD-950-100.000</td>
<td>Crystek</td>
</tr>
</tbody>
</table>

- A XO is chosen based on cost constraints and due to the required phase noise performance, according to simulation results in Figure 4-2.
- A PLL chip from ADI was chosen based on familiarity of programming interface and sufficiently low internal noise floor.
- The VCO and x4 multiplier are chosen based on availability and satisfactory phase noise performance.
- Output amplifier is chosen based on the needed output power and availability. It has saturated power of 19 dBm, which is close to the desired value of 18 dBm (Section 4.2).
• Op-Amp is chosen for its smallest noise (1.1 nV/√Hz) with at least 12 V rails required for tuning of the VCO.

4.4 PLL LOOP FILTER DESIGN

Based on simulation, using measured VCO phase noise, and datasheets for the rest of the components, the following plot shows contributions of Reference/PLL, VCO and loop filter on the overall phase noise of the synthesizer:

![Figure 4-2 PLL Phase Noise Simulation at 57.6 GHz.](image-url)
By setting the 3 dB bandwidth of the PLL loop to around 110 KHz, as presented on Figure 4-2, an optimal integrated phase noise of 2.5° is achieved, much less than the requirement of 4° derived in Chapter 3.

Due to a maximum tuning voltage of the VCO of 10V and a Charge Pump voltage of 5 V, the loop topology has to include an active component. An active device is usually implemented using a transistor or an Operational Amplifier (Op-Amp). Due to high power supply noise rejection, high input impedance, and low offset voltage a low noise Op-Amp is chosen to scale the voltage to proper range instead of transistor. The Op-Amp noise (1.1 nV/√Hz) is found in simulation to have a small contribution to the overall noise. To allow for Op-Amp power supply rail room and PLL tuning voltage overshoot, the supply voltage is chosen to be 15V (10V needed for the VCO).

The resistors in the PLL loop filter introduce in-band noise and therefore need to be minimized. When reducing the loop resistors, while keeping the loop bandwidth constant, the loop capacitors would have to increase. Due to size limitations, the footprint chosen for the biggest loop capacitor corresponds to a 0603 surface mount package. In this footprint capacitors values are limited to a maximum of approximately 2 μF (at rated voltage more than 15V).

The next section will show how to optimize loop parameters such as damping factor and natural frequency in order to get the best integrated phase noise.

4.5 PLL LOOP FILTER OPTIMIZATION

If a specific VCO has been selected for a given output frequency and a frequency step size, a reference source and a PLL chip (containing N, R -dividers, and PFD) that would meet the phase noise specification with a margin. Next, we would like to know the following:

1. The Loop Filter (LF) topology and LF order that is sufficient for minimization of the overall phase noise.
2. Component values of the LF which are optimal for minimization of the overall phase noise of the PLL.

4.5.1 LOOP FILTER ORDER AND TOPOLOGY

From literature [18][19][20] it is clear that a 2\textsuperscript{nd} order LF is sufficient for integer-N PLLs and high PFD frequencies. Higher order loops tend to have worse stability performance and while having no positive effect on the overall phase noise (in fact increasing it by small amount as will be shown). Since the present synthesizer is an integer PLL with 100 MHz PFD frequency there no need for higher than 2\textsuperscript{nd} order LF for spurious considerations. A common integrator-lead RC filter [20] is chosen:

![Second Order LF used in the Synthesizer.](image)

4.5.2 LOOP FILTER OPTIMIZATION WITH NEGLIGIBLE RESISTOR NOISE

VCO closed-loop noise transfer function for the 2\textsuperscript{nd} order LF on Figure 4-3 is:

\[
\varphi_{\text{noise-out}} = \frac{s^2 \cdot \left( s \frac{2\zeta}{\omega_n} + 1 \right)}{s^2 \cdot \left( s \frac{2\zeta}{\omega_n} + 1 \right) + \left( 2\zeta \omega_n s + \omega_n^2 \right)}
\] (4.5.1)

Where \( r = C1/C2 >> 1 \) (an approximation is used \( C_2 \sim C_1 || C_2 \) for \( C_2 << C_1 \))
Reference/PLL-chip closed-loop noise transfer function for 2\textsuperscript{nd} order loop:

\[
\frac{\Phi_{\text{noise-out}}}{\Phi_{\text{REF-noise}}} = \frac{2\zeta w_n \cdot s + w_n^2}{s^2 \left( s \frac{2\zeta}{r w_n} + 1 \right) + 2\zeta w_n s + w_n^2} \quad (4.5.2)
\]

For now, the VCO phase noise is assumed to roll off at 20dB/decade at offsets around the loop 3dB frequency. Reference/PLL phase noise is assumed to be predominantly thermal (flat spectral density) around the loop 3dB frequency. This assumption is usually valid but there are cases where Reference/PLL phase noise has a small slope (< 10 dB/dec).

Simulation are performed in MATLAB by sweeping \(\omega_n\), \(\zeta\) and \(\tau\). The following graphs show these sweeps for one of the variables chosen such that in minimizes the integrated phase noise:

![Graph showing optimal \(\omega_n\) for various \(\zeta\) values. C1/C2 = 5, 10, 20, 30.](image-url)

Figure 4-4. Optimal \(\omega_n\) for various \(\zeta\). C1/C2 = 5, 10, 20, 30.
Figure 4-5. Integrated Phase Noise vs. ϶’s for various C1/C2 ratios.

4.5.3 COMPARISON TO LITERATURE

The following figure illustrates the selection of optimal noise bandwidth of the loop filter to minimize integrated phase noise, as shown in [20]:

Figure 4-6. Equivalent (two-sided) Noise Bandwidth for 2\textsuperscript{nd} order PLL.
From Figure 4-6 we see that the optimal $\zeta$ for minimal noise bandwidth of 2\textsuperscript{nd} order LF is 0.5 while we get about 1.3 (2\textsuperscript{nd} order LF approximation where $C_2$ is assumed to be negligible). This discrepancy comes from the fact that in [20] the author is minimizing the integrated closed-loop phase noise of the reference while the presented analysis in this thesis takes into account the VCO phase noise as well. Therefore, the results reported on Figure 4-5 are expected to be more accurate than the one reported in [20], at least for the VCO phase noise in a region with a slope of 20 dB/dec. The next section presents a more generic analysis for the various VCO slope regions (10 – 30 dB/dec) and considers phase noise introduced by the LF resistor as well.

### 4.5.4 LF Optimization With the Resistor Noise for Various VCO Slopes

According to the Leeson equation, the VCO slope can vary from 10 to 30 dB/dec [28], The place of intersection of the Reference/PLL and VCO phase noise determines the slope of the VCO used in calculations, as illustrated:

![Figure 4-7. VCO Phase Noise Intersecting PLL/Ref. Phase Noise at Points with Various VCO Slopes.](image)

Large damping factors require increased resistor values which increases the noise introduced by the loop filter. In some cases it’s hard to reduce PLL open loop gain to
reduce the resistor value and phase noise introduced by the loop resistor becomes significant. In this case we need to incorporate loop filter noise into the general loop optimization theory done in previous chapter.

The loop resistor can be found using the following equation \[19\] \[27\]:

\[
R = \frac{2\zeta w_n}{K_{loop}}, \quad \text{where} \quad K_{loop} = \frac{IK_{VCO}}{2\pi N}
\] (4.5.3)

Therefore, one needs to look at what level of noise introduced by loop filter can be tolerated without significantly affecting overall noise.

The noise introduced by the resistor is filtered by the following transfer function \[27\]:

\[
i_{n,LPF} = \frac{1}{R} \cdot \frac{v_n s}{s + \frac{1}{RC_2}}, \quad \text{where} \quad v_n = \sqrt{4kTR}
\] (4.5.4)

This resistor noise current is applied to \(C_2\) which leads to the voltage on the VCO tuning port which is calculated as follows:

\[
v_{n-vtune} = \frac{1}{sC_2} \cdot i_{n,LPF} = \frac{1}{RC_2} \cdot \frac{v_n}{s + \frac{1}{RC_2}} = \frac{1}{RC_2} \cdot \sqrt{4kTR} \cdot \frac{1}{s + \frac{1}{RC_2}}
\] (4.5.5)

Which simplifies to:

\[
v_{n-vtune} = \sqrt{\frac{8kT}{K_{loop}}} \cdot \frac{\sqrt{\zeta w_n}}{s + \frac{2}{r w_n} + 1}, \quad \text{where} \quad r = \frac{C_1}{C_2}
\] (4.5.6)
This is a low pass function with 3dB frequency defined by 1/RC<sub>2</sub>. This noise voltage on the VCO tuning port is converted to phase noise using VCO transfer function \( \frac{K_{VCO}}{s} \) and closed-loop transfer function of the PLL to produce the following phase noise contribution of the loop filter resistor to the overall phase noise in a closed loop:

\[
\varphi_{LPF} = \frac{K_{VCO}}{s} \sqrt{\frac{8kT}{K_{loop}}} \cdot \frac{s^2 \sqrt{\zeta \omega_n}}{s^2 \left( s - \frac{2\zeta}{\omega_n} + 1 \right) + \left( 2\zeta \omega_n s + \omega_n^2 \right)}
\]

By differentiating the denominator and equating to zero, the peak of the transfer function happens at \( \omega_{1,2}^2 = (C_1 \pm C_2)\omega_n^2 \) where \( C_1 \) and \( C_2 \) are functions of \( \zeta \) and \( r \). In other words the peak of the LF transfer function will move with \( \omega_n \) in linear fashion. Now we need to find out how gain at the peak changes with \( \omega_n \). Substituting \( \omega_{1,2} \) into the equation (4.5.7) we can see that the peak amplitude of the transfer function is proportional to \( 1/\sqrt{\omega_n} \).

Now we can normalize the frequency of the LF transfer function to the VCO - PLL/Ref. intersection frequency while taking into account the change in amplitude of the LF phase noise. The phase noise transfer function is normalized in frequency as \( \omega_n \rightarrow \omega_n/\omega_{xsect} \) and amplitude as follows:

\[
\varphi_{LPF} = \varphi_{LPF\ norm} \cdot K_r
\]

To be more generic, a normalization of the LF noise would have to take into account how close it gets to the in-band noise level. For this purpose it’s necessary to normalize LF phase noise to the in-band phase noise level, which we call \( \varphi_{REF-noise} \). Combining all of the normalization factors into one, we define LF phase noise normalization factor \( K_r \):

\[
K_r = \frac{K_{VCO}}{\varphi_{REF-noise} \cdot \sqrt{K_{loop} \omega_{xsect}}}
\]

Where \( \omega_{xsect} \) is the VCO - PLL/Ref. phase noise crossover offset frequency.
Finally, we can plot the overall phase noise with fully generic amplitude and frequency parameters of a PLL and get $\omega_n$ and $\zeta$ for optimal overall phase noise for given $Kr$ and $r$ ($r=C_1/C_2$). After using (4.5.3) and (4.5.10) we can use the graphs below and get optimal $\omega_n$ and $\zeta$, after which we can get $C_1, C_2$, and $R$ from (4.5.3) and [27]. The following plots show optimal $\omega_n$, damping factor $\zeta$ for minimum integrated phase noise and the normalized integrated phase noise for various normalization factors $Kr$ and capacitor ratios $r$.

![Graph showing optimal $\omega_n$, damping factor $\zeta$ for minimum integrated phase noise and the normalized integrated phase noise for various normalization factors $Kr$ and capacitor ratios $r$.](image)

Figure 4-8. $\omega_n$ (norm. to $\omega_{vco}$) for Optimal Phase Noise vs. Capacitance Ratio $r=C_1/C_2$, for Different VCO Slopes.
Figure 4-9. Damping factor, $\zeta$, for Optimal Phase Noise vs. Capacitance Ratio $r=C_1/C_2$, for Different VCO Slopes.

Figure 4-10. Integrated Phase Noise for Optimal $\omega_n$ and $\zeta$ vs. Capacitance Ratio $r=C_1/C_2$, for $Kr < 10^9$, for Different VCO Slopes.
The plot of Figure 4-10, suggests that picking a value of $r$ less than commonly used value of 10 results in sharp increase in the integrated phase noise even with optimal $\omega_n$ and $\zeta$. Values of $r$ bigger than 10 results in roughly 10% improvement in the integrated phase noise, but at a cost of the increased level of reference spurs as the 2\textsuperscript{nd} pole is moved to higher frequency. The proposed synthesizer is using $r$ of 10, which means that the integrated phase noise could be improved from 2.8° to 2.5°, which is not really a big difference in terms of SNR degradation (about 0.2 dB). Degradation of the phase noise due to the reference spurs is not considered here since the PFD frequency is 1000 times bigger than the loop 3 dB frequency.

Next we explore the effect of the LF resistor noise on the overall phase noise. The figures below show phase noise degradation as a function of $Kr$ for VCO slope of 20dB/dec and capacitance ratios, $r$, of 10 and 20.

![Figure 4-11. Integrated Phase Noise for Optimal $\omega_n$ and $\zeta$ vs. $Kr$, for VCO Slope of 20dB/dec.](image)

Figure 4-11. Integrated Phase Noise for Optimal $\omega_n$ and $\zeta$ vs. $Kr$, for VCO Slope of 20dB/dec.
Using the general design procedure derived in previous section, the loop filter is designed with the selected Reference and VCO (Table 4-2). From the VCO and PLL datasheets, and using equations (4.5.3), (4.5.9), (4.5.10), Figure 4-8, and Figure 4-9 the optimal PLL Loop Filter parameters are summarized in Table 4-3.

Table 4-3. PLL Loop Filter Parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F_{out}$</td>
<td>14.4</td>
<td>GHz</td>
<td>$K_r$</td>
<td>1.54 e9</td>
<td></td>
</tr>
<tr>
<td>$f_{exec}$</td>
<td>65</td>
<td>KHz</td>
<td>$\omega_n$</td>
<td>0.56 $\times \omega_{exec}$</td>
<td>rad/s</td>
</tr>
<tr>
<td>VCO slope</td>
<td>20</td>
<td>dB/dec</td>
<td>$\zeta$</td>
<td>0.9</td>
<td></td>
</tr>
<tr>
<td>$K_{VCO}$</td>
<td>2$\pi$ 200</td>
<td>MHz/V</td>
<td>$f_n$</td>
<td>48.1</td>
<td>KHz</td>
</tr>
<tr>
<td>$K_{LOOP}$</td>
<td>5208</td>
<td></td>
<td>$f_{3dB}$</td>
<td>112</td>
<td>KHz</td>
</tr>
<tr>
<td>$r$</td>
<td>10</td>
<td></td>
<td>$C_1$</td>
<td>57</td>
<td>nF</td>
</tr>
<tr>
<td>$\Phi_{REF-noise}$</td>
<td>-83</td>
<td>dBc/Hz</td>
<td>$C_2$</td>
<td>5.7</td>
<td>nF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$R$</td>
<td>100</td>
<td>$\Omega$</td>
</tr>
</tbody>
</table>

4.6 Low-Noise Power Supply Design

Low noise power supply design is critical for PLLs, as passive filtering is not enough because of the large current consumption of the VCO. Noise in the power supply of the VCO (and other components) modulates the RF signal, such that it gets mixed, producing additive phase noise. This section will explore the effects of power supply noise on the VCO and the reference XO. The noise specification is derived for the selected VCO and Reference (Table 4-2) starting with the VCO.

4.6.1 Effect of the Power Supply Noise on the VCO

The Leeson equation, with added tuning diode effect [28], describes how the phase noise of the VCO is affected by various VCO parameters:
\[ L(f_m) = \left[ 1 + \frac{1}{f_m^2} \left( \frac{f}{2QL} \right)^2 \right] \frac{FKT}{2P_{sav}} \left( 1 + \frac{f_c}{f_m} \right) + \frac{2kTRK_0^2}{f_m^2} \] (4.6.1)

Where \( \frac{2kTRK_0^2}{f_m^2} \) is the contribution due to power supply or tuning diode noise, \( R \) is equivalent noise resistance of the tuning diode or power supply noise, \( K_0 \) is the tuning sensitivity or pushing value in Hz/V, \( f_m \) is offset frequency, \( f_c \) is the center frequency.

With power supply noise density given by \( \nu_n = \sqrt{4kTR} \left[ V/\sqrt{Hz} \right] \) and tuning diode phase noise being the same in both cases (cancelled), the added phase noise is then:

\[ \Delta L(f_m) = \frac{\nu_n^2K_0^2}{2f_m^2} \] (4.6.2)

Given acceptable phase noise degradation, \( dL_{\text{dB}} \), due to power supply noise, the maximum voltage noise density of the power supply is calculated as follows:

\[ \frac{\nu_n^2K_0^2}{2f_m^2} = (10^{dL_{\text{dB}}/10} - 1) \cdot L(f_m) \] (4.6.3)

After rearranging, this leads to:

\[ \nu_n = \frac{f_m}{K_0} \sqrt{2(10^{dL_{\text{dB}}/10} - 1) \cdot L(f_m)} \] (4.6.4)

Where \( L(f_m) \) is phase noise of the VCO on linear scale, \( f_m \) is offset frequency in Hz, \( K_0 \) is VCO pushing coefficient in Hz/V.

Applying this to the synthesizer and using datasheet of the VCO: \( K_0=30 \text{ MHz/V} \), at around \( f_m=100 \text{ KHz} \), \( L(f_m) \) is -105 dBc/Hz or \( 3.16 \cdot 10^{-11} \). Then for 1 dB degradation in PN, \( L(f_m) \) would be \( 3.98 \cdot 10^{-11} \), and the required power supply noise density is:
\[ \nu_n = \frac{10^5 \text{Hz}}{3 \cdot 10^7 \text{Hz/V}} \sqrt{2 \cdot (10^{0.1} - 1) \cdot 3.98 \cdot 10^{-11}} = 15nV/\sqrt{\text{Hz}} \] 

(4.6.5)

Therefore the power supply noise density should be less than 15nV/\sqrt{\text{Hz}} in order to have less than 1dB of degradation in the phase noise of the VCO (around 100 KHz offset). This required power supply noise density is accurate and constant where VCO phase noise slope is 20 dB/dec. This can be checked easily by substituting 100-times less phase noise and increasing \( f_m \) by 10. If VCO slope is different from 20 dB/dec then \( \nu_n \) needs to be calculated at different offset frequencies of interest. Note: this added phase noise due to power supply noise will be filtered out by closed loop transfer function of the VCO. Therefore power supply noise will have the most noticeable effect around natural frequency of the PLL where the gain of the VCO closed loop transfer function is biggest [20].

The voltage noise of the voltage regulator (Linear Tech. LT3085) followed by the common-base active filter (see Appendix for schematic) is simulated in LTspice free Spice simulator with accurate model of the voltage regulator from Linear Technologies with the resulting voltage noise power density:

![Figure 4-12. Voltage Noise of the Power Supply.](image-url)
Since VCO phase noise is highest around the cross over frequency and continues to be directly added to the VCO phase noise after it, frequencies bigger than 10 KHz are most important. The results of noise simulation of the power supply show a noise density of $4nV/\sqrt{Hz}$ after 10 KHz, which is much lower than the required $15 nV/\sqrt{Hz}$.

4.6.2 **Effect of the power supply noise on the Reference**

Reference XO has a very high Q resonator with very small pushing, with phase noise of $-157$ dBc/Hz at 10K or $2 \times 10^{-16}$ 1/Hz. For 1 dB degradation in phase noise the required phase noise should be: $5 \times 10^{-17}$ 1/Hz. Based on similar oscillators, pushing factor, $K_0$, is assumed to be around 10 ppm or 1 KHz/V. Using the same procedure as with the VCO, the required power supply noise density has to be less than $200 nV/\sqrt{Hz}$, which is not a problem with the noise presented on Figure 4-12.

4.7 **Conclusions**

The synthesizer is designed using off-the-shelf components to meet the $4^\circ$ integrated phase noise requirement, with predicted integrated phase noise of $2.5^\circ$. PLL loop filter optimization procedure is presented and applied to the design of the presented synthesizer providing optimal loop filter component values for minimum integrated phase noise. The noise specification of the power supply for the synthesizer is derived based on the effect of voltage noise on the VCO phase noise. Next two chapters show how the synthesizer is implemented.
Chapter 5. MHMIC PACKAGING

The amplifier and multiplier section of the synthesizer has 10 bias lines plus about 15 ground contacts coming to an area of about 15 mm$^2$. For this kind of signal density the PCB would have to have many layers (~ 8) and require very small via holes, which would increase the cost dramatically. The capacitive decoupling on power supply and bias lines is required to be as close to the chips as possible (30 mil max), as explained in the amplifier and multiplier datasheets. This restriction comes from the fact that the signal frequencies that need to be decoupled are between 14 and 64 GHz. The manufacturer suggests that the bias lines of the amplifier and multiplier should have 100 pF single layer decoupling capacitors with resonance above 15 GHz. The assembly diagrams for the 60 GHz amplifier and multiplier are shown below:
Figure 5-1. Manufacturer-Recommended Assembly of the x4 Multiplier.
Figure 5-2. Manufacturer-Recommended Assembly of the Amplifier.

The synthesizer is assembled on a low-cost Miniature Hybrid Microwave Integrated Circuit (MHMIC) process, which uses an Alumina substrate, developed at the Communications Research Centre Canada (CRC). This packaging solution was chosen over PCB (such as Rogers’ Duroid) because of the fine resolution necessary for the large number of bias lines of the multiplier and amplifier chips. Additionally, MHMIC packaging offers proven performance at frequencies at and above 60 GHz, availability, low cost and flexibility of manufacturing process. The process uses lithography to define layers, metal deposition by sputtering, SU-8 dielectric and photoresist deposition. This allows superior trace resolution of 5μm and perfect surface/edge trace roughness. Another advantage of MHMIC, is that the process comes with standard integrated MIM capacitors, thin-film resistors, planar inductors, and various transmission lines (CPW, microstrip, slot-lines).
5.1 MHMIC Layer Definition

The layer stack-up of the process:

![Layer Stack-up of MHMIC Process](image)

The layers of the MHMIC process are: ME1, ME2 – 4 μm gold metal, WIN – SU8\(^2\) dielectric layer (\(\varepsilon_r=4\)), SUB – 400 μm Alumina (Al\(_2\)O\(_3\)) substrate (\(\varepsilon_r=9.6\)). Three masks are used in manufacturing of the MHMIC package. One for defining features of ME1, by photo-resist deposition, UV exposure and etching, one for dielectric layer (WIN) patterning, and one for ME2 deposition /etching.

5.2 Assembly and Layout

Surface mount components are attached to the package with silver epoxy and cured. The bare-die components (x4 multiplier and amplifier) are attached to the package with silver epoxy, cured, and then wire-bonded with wire ribbons. The holes are drilled in MHMIC package and filled with silver epoxy at the die locations to provide the required thermal dissipation path to underlying heat-sink. The synthesizer output is wire-bonded to a filter outside of the package which, in turn, is wire-bonded to the mixer. The parasitic losses of the wire-bonding were estimated based on ribbon size available to be on order of 1 dB. The reference input is wire-bonded to the PCB containing OCXO, power supplies and micro-controller for programming of the PLL chip.

\(^2\) SU-8 – an epoxy-based negative photo resist
MHMIC layout is shown below with populated components:

Figure 5-4. Populated MHMIC Synthesizer Board. a) Top View of the MHMIC Synthesizer. b) Bare-die Placement on the MHMIC Package of Multiplier (left) and Amplifier (right).
5.3 **THERMAL ANALYSIS**

Thermal analysis needs to be performed in order to investigate the temperature rise due to the power dissipation is above absolute maximum reported in the device datasheet. Heat conduction follows similar laws as current flow: a temperature difference is like voltage difference and heat flow (in Watts) is like current. Just like electrical resistivity, materials are characterized as having a certain thermal conductivity $\sigma$ (W/(K·m)) or resistance $\theta$ (K·m/W). The thermal resistance formula is exactly like for electricity and it is:

$$\Theta = \theta \frac{l}{A}$$  \hspace{1cm} (9.4.1)

Where $\Theta$ is thermal resistance in Kelvin/Watt, $l$ is length, $A$ is cross-sectional area.

Due to problems with drilling of the MHMIC substrate, there is no cavity under the VCO for thermal relief while there are holes under the multiplier and amplifier. The following diagram illustrates the layers through which heat flows for VCO and multiplier/amplifier:

![Thermal-Flow Diagram for VCO, Multiplier and Amplifier.](image)

Figure 5-5. Thermal-Flow Diagram for VCO, Multiplier and Amplifier.
The MHMIC synthesizer has components that consume significant amount of current. The following table illustrates the power used by the biggest contributors:

Table 5-1. MHMIC Synthesizer Power Consumption.

<table>
<thead>
<tr>
<th>Power, mW</th>
<th>Device</th>
<th>Manufacturer PN</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,625</td>
<td>14-15 GHz VCO</td>
<td>HMC398QS16G</td>
<td>Hittite</td>
</tr>
<tr>
<td>1,100</td>
<td>50-66 GHz power amplifier</td>
<td>HMC-ABH241</td>
<td>Hittite</td>
</tr>
<tr>
<td>481</td>
<td>54-64 GHz output x4 Multiplier</td>
<td>HMC-XDH158</td>
<td>Hittite</td>
</tr>
<tr>
<td>55</td>
<td>PLL</td>
<td>ADF4106</td>
<td>ADI</td>
</tr>
<tr>
<td>3,261</td>
<td>TOTAL</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The thermal resistance of a stack of different materials is calculated just like resistance in electrical circuit, as a series connection. The following table with material properties will be used to calculate thermal resistance for VCO and Amplifier/Multiplier:

Table 5-2. Thermal Resistance of Materials used.

<table>
<thead>
<tr>
<th>Material</th>
<th>Conductivity, W/m/K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silver Epoxy</td>
<td>2.5</td>
</tr>
<tr>
<td>Alumina</td>
<td>25</td>
</tr>
<tr>
<td>Brass</td>
<td>110</td>
</tr>
</tbody>
</table>

Assuming that the Silver epoxy thickness is 1 mil (worst case), then Silver epoxy thermal resistance is 10 K-mm²/W. Alumina substrate thickness is 250 μm, then its thermal resistance is 10 K-mm²/W. According to the VCO datasheet, the VCO thermal resistance is 24 K/W (junction to case). The natural air convection transfer coefficient is about 20 W/m²/K (5-25), therefore for the housing which has surface area of 60 cm², the worst case thermal resistance from the housing to air is 8 K/W. Brass resistance for the 5 mm thick housing would be 45 K-mm²/W. Brass housing resistance consists of vertical column resistance + side resistance which results in total housing area being the radiator.
Side resistance is approximated as side area × half length of the housing: \( \Theta_{\text{HOUSING}} = \frac{1}{1/(110 \text{ W/m/K} \cdot 5\text{mm} \cdot 20\text{mm}/38.1\text{mm})} = 3.4 \text{ K/W} \).

### 5.3.1 VCO

Since the active thermal area of the VCO is around 25 mm\(^2\). Then, the overall thermal resistance of VCO is: 
\[
\Theta_{\text{VCO}} = 24 \text{ K/W} + (10 + 10 + 10 + 45) \text{ K-mm}\(^2\)/W /25 \text{ mm}\(^2\) + 3.4 K/W + 8 K/W = 38.4 \text{ K/W}.
\]
Due to 1.63 W dissipation, the temperature rise is 1.63 W \cdot 38.4 \text{ K/W} = 62 \degree\text{C}, and the final temperature is 87 \degree\text{C}, slightly higher than maximum specified 85 \degree\text{C}.

### 5.3.2 AMPLIFIER

Because active area of the Amplifier is 4.5 mm\(^2\), the overall thermal resistance of the amplifier is: 
\[
\Theta_{\text{AMP}} = 24 \text{ K/W} + (10 + 45) \text{ K-mm}\(^2\)/W /4.5 \text{ mm}\(^2\) + 7.5 K/W + 8 K/W = 28 K/W.
\]
Due to 1.1 W dissipation, the temperature rise is 1.1 W \cdot 28 K/W = 31 \degree\text{C}, and the final temperature is 56 \degree\text{C}, which meets the spec.

### 5.3.3 MULTIPLIER

Calculation for the Multiplier follows the same procedure with resultant thermal resistance, \( \Theta_{\text{MULT}} \), of 60.6 K/W, and the corresponding temperature rise is 29 \degree\text{C}, with the die temperature of 54 \degree\text{C}, which meets the spec.
Chapter 6. PCB PACKAGING

The MHMIC synthesizer board has 16 DC, 2 RF, and 4 digital signal lines. The large number of DC lines with different voltages requires many power supplies. It's impractical to provide 16 different voltages from laboratory power supplies. Therefore, a suitable solution has to have local power supplies in the synthesizer assembly. Due to the layout of the MHMIC, a connectorized solution would have been a lot more complicated, as it would require additional layers of PCB and more complex routing on the MHMIC board. The proposed solution uses a PCB with MHMIC board connected with bond wires to the PCB which provides power, digital control signals, and the PLL Reference.

The PCB contains power supplies, 100 MHz reference, and Microcontroller (MCU) with 16 MHz clock. Due to low frequency nature of the components on the PCB and considering that the 100 MHz signal is strong 3.3V TTL there is no need to have a high quality substrate for the PCB. For these reasons, the cheapest, and widely available, FR4 PCB substrate is chosen.

Figure 6-1. Side-view Diagram of the Final Assembly.
6.1 PCB Layer Stackup

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder mask</td>
<td>0.5mil</td>
<td></td>
</tr>
<tr>
<td>Top (Signal)</td>
<td>Copper 1oz (1.4mil)</td>
<td></td>
</tr>
<tr>
<td>FR4 dielectric</td>
<td>14mil</td>
<td></td>
</tr>
<tr>
<td>Layer 2 (GND)</td>
<td>Copper 1oz (1.4mil)</td>
<td></td>
</tr>
<tr>
<td>FR4 dielectric</td>
<td>28mil</td>
<td></td>
</tr>
<tr>
<td>Layer 3 (Signal)</td>
<td>Copper 1oz (1.4mil)</td>
<td></td>
</tr>
<tr>
<td>FR4 dielectric</td>
<td>14mil</td>
<td></td>
</tr>
<tr>
<td>Bottom (GND)</td>
<td>Copper 1oz (1.4mil)</td>
<td></td>
</tr>
<tr>
<td>Solder mask</td>
<td>0.5mil</td>
<td></td>
</tr>
</tbody>
</table>

Figure 6-2. Stack-up of the FR4 Board.

6.2 PCB Implementation

Figure 6-3. Full Assembly of the Synthesizer. Perspective View.
Figure 6-4. Full Assembly of the Synthesizer. Top View with Labels.
Chapter 7. **MEASUREMENTS**

7.1 **MEASUREMENT SETUP AND CALIBRATION**

The experimental setup for the synthesizer assembly consists of power supply, Signal Source Analyser (Rohde & Swartz FSUP), and mm-Wave external mixer:

The synthesizer assembly is designed to be reprogrammable from USB, but in its present configuration the frequency switching is not implemented and the output frequency is set at 57.6 GHz. The cable losses are measured using a network analyzer, and mixer conversion loss is measured with a signal generator, a spectrum analyzer and a power meter. Firstly, in order to optimize the PLL loop filter, and eliminate power supply issues, the open-loop phase noise of the VCO is measured, then the overall PLL phase noise is measured with passive loop filter, and finally output spectrum of the synthesizer is presented.
7.2 OPEN LOOP VCO PHASE NOISE MEASUREMENT

The open-loop phase noise of the Hittite 14-15 GHz VCO is measured in-circuit, by disconnecting power supplies, Vtune, and RF output. Power supply and Vt is provided from the R&S FSUP, while the RF is taken from the VCO using a “pig-tail” coaxial cable (see Figure 7-2) with shield connected to the ground plane of the MHMIC.

Figure 7-2. "Pig-tail" coaxial cable connection.

A “pig-tail” coaxial cable is required since the VCO was not available in a stand-alone evaluation board. Due to the “pig-tail” connection the output power is not accurate, but within 10dB of the actual power. The following plot shows the measurement of the VCO phase noise in open-loop:
As can be seen above the VCO output power from the "pig-tail" connection is -2.2 dBm, and after accounting for the loss in "pig-tail" and cable connection the actual output power is +4dBm. The measured phase noise is noticeably worse than the specified on the datasheet, as can be seen from the following comparison table:
Table 7-1. VCO Phase Noise - Measurements vs. the Datasheet.

<table>
<thead>
<tr>
<th>Frequency Offset, KHz</th>
<th>Datasheet, dBc/Hz</th>
<th>Measured, dBc/Hz</th>
<th>Difference, dBc/Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-42</td>
<td>-42</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>-74</td>
<td>-72</td>
<td>2</td>
</tr>
<tr>
<td>100</td>
<td>-105</td>
<td>-101</td>
<td>4</td>
</tr>
<tr>
<td>1000</td>
<td>-130</td>
<td>-128</td>
<td>2</td>
</tr>
<tr>
<td>10000</td>
<td>-140</td>
<td>-137</td>
<td>3</td>
</tr>
</tbody>
</table>

As we see from above table the VCO phase noise is worse by about 3 dB on average. The VCO required to be assembled in several occasions (4 times) due to difficulties during surface-mount assembly. As discussed in thermal analysis Section 5.3, the VCO junction temperature exceeds the maximum limit by 2 °C, and could be more if assumptions are off. The measured case temperature is about 50 °C, so it’s not clear what is the junction temperature from thermal measurements. The high failure rate could also be due to poorly done silver epoxy underneath the package, again, increasing junction temperature. Another potential reason could be that, initially, there was a small instability in the 5V voltage regulator supplying the VCO, but only about 100 mVp-p, 1 MHz.

7.3 SYNTHESIZER PHASE NOISE MEASUREMENT

The synthesizer phase noise is measured at 57.6 GHz with a Rohde & Schwarz FSUP SSA and an external V-band mixer (20.6 dB conversion loss with cables). The following is the synthesizer phase noise measurement plot, followed by a measurement vs. simulation comparison plot:
Figure 7-4. Phase Noise Measurement of the Synthesizer at 57.6 GHz with a passive loop filter.

The plot above shows phase noise of the full synthesizer assembly, locked to the internal 100 MHz reference with a passive 3rd order PLL loop filter. The measured integrated phase noise is 2.8° (integrated between 1 KHz and 30 MHz offsets). After accounting for cable and mixer losses, the output power is +1 dBm. The output power is +4 dBm as measured by the power meter (which takes into account most of the harmonic power as well). Figure 7-5 shows comparison of measured and simulated phase noise:
Figure 7-5. Measured and Simulated Phase Noise at 57.6 GHz with Simulated Main Phase Noise Contributors.

Simulated closed-loop phase noise includes contributions of VCO, Reference/PLL (Ref/PLL), Loop Filter (LF) and overall phase noise (Total sim). The difference between measurement and theory is summarized in Table 7-2:

Table 7-2. Comparison of Measured and Simulated Phase Noise.

<table>
<thead>
<tr>
<th>Frequency Offset, KHz</th>
<th>Simulated, dBC/Hz</th>
<th>Measured, dBC/Hz</th>
<th>Difference, dBC/Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-82.1</td>
<td>-71.0</td>
<td>11.1</td>
</tr>
<tr>
<td>10</td>
<td>-81.9</td>
<td>-79.7</td>
<td>2.2</td>
</tr>
<tr>
<td>100</td>
<td>-79.4</td>
<td>-81.0</td>
<td>-1.6</td>
</tr>
<tr>
<td>1000</td>
<td>-82.4</td>
<td>-83.0</td>
<td>-0.6</td>
</tr>
<tr>
<td>2000</td>
<td>-113.0</td>
<td>-111.6</td>
<td>1.4</td>
</tr>
<tr>
<td>10000</td>
<td>-120.3</td>
<td>-119.0</td>
<td>1.3</td>
</tr>
<tr>
<td>30000</td>
<td>-130.0</td>
<td>-125.0</td>
<td>5.0</td>
</tr>
</tbody>
</table>

Integrated, ° 2.5  2.8  0.3
From measured phase noise plot on Figure 7-5 and comparison Table 7-2 we can see that the measured phase noise at 1 KHz is worse by 10 dB. This could be explained by a higher power supply noise at 1 KHz. As can be seen in power supply design Section 4.6, the power supply noise goes up at 1KHz, although it’s not enough to cause such a large influence the frequency at which it happens indicates a possible source. Also, the datasheet for the ADF4106 PLL has no information on low frequency-offset phase noise degradation (such as 1/f noise), aside from a figure of merit which indicates a flat noise floor.

The discrepancy at higher offset is due to a high attenuation in the RF chain which increases the thermal noise floor significantly:

Figure 7-6. Phase Noise Degradation due to Excess Attenuation.

From the R&S FSUP datasheet, the internal noise floor is about -146 dBm (attenuation setting of 0dB, LO/IF port). This, coupled with a signal power of -19dBm at FSUP, results in a phase noise floor of -127 dBc/Hz at 10 MHz offset. Combining this noise floor with the open loop VCO measurement of -137 dBc/Hz, the predicted phase noise would be -126.6 dBc/Hz. The measured result is -125 dBc/Hz, which is within the accuracy of the measurement and calibration from the predicted result.
7.4 COMPARISON TO PUBLISHED RESULTS

The synthesizer performance is primarily focused on phase noise, and as was shown in Chapter 3, the integrated phase noise is what determines the SNR degradation of the whole system. Therefore, it is interesting to compare the measured phase noise to results published literature. At the time of wiring, to my knowledge, there is only one System-on-Package (SOP) publication focused on 60 GHz synthesizer with reasonable phase noise, the rest are mainly System-On-Chip (SOC). Comparing SOC and SOP is not very appropriate, as SOC doesn’t have the luxury of integration of various semiconductor technologies or the high power consumption. None the less it’s interesting to see what kind of phase noise is achievable in SOC vs. SOP. The following table compares some of the synthesizers and transceivers operating close to the 60 GHz band:

Table 7-3. Comparison of Measured Results.

<table>
<thead>
<tr>
<th>Publication, SoC or SoP</th>
<th>Phase Noise at 1 MHz offset, dBC/Hz</th>
<th>Integrated Phase Noise (RMS jitter)(^a)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[29] May 2008, SoC</td>
<td>-91.6</td>
<td>5°</td>
</tr>
<tr>
<td>[30] Nov. 2010, SoC</td>
<td>-86.5</td>
<td>8°</td>
</tr>
<tr>
<td>[31] Feb. 2008, SoC</td>
<td>-86.8</td>
<td>58°</td>
</tr>
<tr>
<td>This work, SoP</td>
<td>-111.5</td>
<td>2.8°</td>
</tr>
</tbody>
</table>

\(^a\) Integrated from 1 KHz to 30 MHz. Based on piece-wise linear interpolation from phase noise plots, normalized to 57.6 GHz.
7.5 OUTPUT SPECTRUM

Output of the synthesizer is measured on the R&S FSUP at 57.6 GHz in 1 GHz span to show the level of the reference spurs.

![Output Spectrum Diagram]

Figure 7-7. Output Spectrum of the Synthesizer at 57.6 GHz.

Synthesizer output spectrum contains strong spurious signals at the 100 MHz reference frequency grid. There are several mechanisms for this:

- Reference signal coupling back from the PLL to the VCO through the divider port, and to the VCO output, creating grid of 400 MHz and weaker 100 MHz one.
• Power supply lines picking up 100 MHz and harmonics and modulating VCO, Multiplier and amplifier. Although there is by-pass capacitors there would still be some coupling.

• Radiation from routing of 100 MHz, coupling to RF lines and power supply lines.

• 100 MHz and harmonics coming from the PLL chip through the loop filter, to the Vtune of VCO. The loop filter has about 100dB attenuation at 100MHz, so most likely it’s coupled to the Vtune through radiation.

• Long gate-bias lines of multiplier and amplifier are quite long, although they have 27 pF decoupling capacitors, some of the 100 MHz radiation still couples.

During the tuning of the bias voltages of the amplifier it was found that for some threshold gain the spurs grow until the amplifier starts showing a spectrum which looks like injection locked oscillation at another frequency. This suggests that, probably, the gate-bias line of the amplifier is subjected to strong reference pickup and at some point, due to gain of the amplifier, starts oscillation.
Chapter 8. **CONCLUSIONS AND FUTURE WORK**

8.1 **CONCLUSIONS**

A cost effective high performance System-on-Package Synthesizer is designed and manufactured based on the derived phase noise requirements from the system analysis. Worst case 802.15.3c signal (Table 3-2) was used for derivation of SNR. The worst case SNR was derived, based on the FCC peak power requirement and Error Control Coding (ECC), to be 18.5 dB for 10 meter link with BER of $10^{-6}$.

The integrated phase noise specification is derived to be $4^\circ$. The derivation process accounts for the effects of phase noise on OFDM, and ECC of the IEEE 802.15.3c standard. Various simulations were performed in Matlab and Simulink to verify that LDPC coding used in the standard brings the required SNR value to 1 dB from the Shannon limit which defined the minimum required SNR to achieve a BER of $10^{-6}$.

A generic 3rd order PLL loop filter optimization procedure was presented for various VCO phase noise slopes, and $C_2/C_1$ capacitor ratios. The effect of the PLL loop filter resistor on the overall phase noise was investigated and a design procedure was presented for optimal design of a PLL loop filter.

A procedure was developed to derive the noise specification of the VCO and reference power supply in order to minimize its effect on the overall phase noise. The noise specification was derived for the selected VCO and clock reference.

The synthesizer has been designed and manufactured using a MHMIC packaging process developed at CRC, with an FR4 PCB motherboard. The debugging and measurement work was performed on the synthesizer and the resulting phase noise was better than the derived requirements. The measured phase noise was -111.5 dBc/Hz (at 1 MHz offset) corresponding to an integrated phase noise of $2.8^\circ$ at 57.6 GHz, resulting in a SNR degradation of only 1.8 dB.
8.2 Future Work

8.2.1 Phase Noise

Phase noise can be improved by selecting a better PLL chip, such as recently released Hittite integer-N PLLs. They offer a noise floor which is 20 dB or so better than Analog Devices ADF4106, but unfortunately Hittite PLLs have several dozen registers (compared to 4 in ADF4106), making it difficult to program.

Even though the OpAmp noise voltage is around 1.1 nV/√Hz, it's still too big if a Hittite PLL was used. A discrete solution can be used if active filter is needed. For example an RF NPN transistor, such as BFR540 can be used. Caution must be taken in order to satisfy the rail performance, as VCO might have the required tuning range. Also, the nonlinearity of the NPN device needs to be compensated digitally my modifying the charge pump current.

Power supply introduced an unexpected phase noise hump around 20 KHz and between 100 KHz and 10 MHz, mainly due to the 5V regulator for the VCO. An extra capacitor of about 2000 μF was added at the output of the regulator, which fixed the problem. This needs to be further investigated, as simulation did not show this effect.

8.2.2 Spurs

To reduce the spurs, it is recommended that the MHMIC bias lines are covered with top metal layer, to reduce radiative coupling. An isolation amplifier should be inserted between the VCO divider port (1.8 GHz) and RF input of the PLL chip to reduce PFD switching coupling back to the VCO. The Reference line must be shielded by routing on internal PCB-layer.
Amplifier power supply tends to create a 1 MHz oscillation if the amplifier current is increased beyond the recommended value on the datasheet (220 mA). If the current exceeds this value, oscillations would show up as a grid of 1 MHz spurs on the output. This needs further investigation, as the voltage regulator simulation shows very good phase margin.

Filter stages can be added between VCO – Multiplier, Multiplier – Amplifier, in order to reduce sub-harmonics of the VCO and some of the 100 MHz reference grid. Amplifier stability needs to be simulated, as at some bias levels the amplifier starts oscillating.
REFERENCES


[22] FCC Regulation 47 CFR 15.255


APPENDIX A
Figure A.1: Schematic of the MMIC Synthesizer.
Figure A-2. Schematic of the PCB motherboard. Part 1
Figure A-3. Schematic of the PCB motherboard. Part 2
Switch between internal XTAL or external

Figure A-4. Schematic of the PCB motherboard. Part 3
VCO, PLL 5V power supply
500mA, 36V in, 1 V drop

Output Amp Drain power supply
500mA, 36V in, 1 V drop

Figure A-5. Schematic of the PCB motherboard. Part 4
Figure A-6. Schematic of the PCB motherboard. Part 5
Figure A-7. MHMIC Synthesizer Layout.
Figure A-8. FR4 PCB layout, TOP layer.
Figure A-9. FR4 PCB layout. Middle layer.
Figure A-10. Simulink diagram of the setup to measure phase noise effect on the encoded signal